Performance Analysis of High Speed Low Power Carry Look-Ahead Adder Using Different Logic Styles

Jagannath Samanta, Mousam Halder, Bishnu Prasad De

Abstract*— A carry look-ahead adder improves speed by reducing the amount of time required to resolve carry bits. It is widely used in any electronic computational devices. In this paper a 4 bit & 8 bit CLA has been implemented using different static and dynamic logic styles such as Standard CMOS, DCVS Pseudo NMOS, PTL & Domino logic style. The performance of the CLA has been measured by comparing the results in terms of propagation delay, power dissipation and their Power Delay Product. The simulation is done with the help of Tanner EDA tool considering the different feature sizes of 150nm, 200nm & 250nm. Result analyses are also carried out for intrinsic and extrinsic load capacitances. This work will helpful for any circuit designer to build any system.

Index Terms*—Carry Look-Ahead Adder, TSpice, Standard CMOS, DCVS, Pseudo NMOS, PTL and Domino logic.

I. INTRODUCTION

Adders are widely used in the generic computer for adding data in the processor [8]. It is also commonly used in various electronic applications e.g. digital signal processing to perform various algorithms like FIR, IIR etc [9]. In past, the major challenge for VLSI designer is to reduce area of chip by using efficient optimization techniques. Then the next phase is to increase the speed of operation to achieve fast calculations. There is lots of research going on to reduce power consumption in VLSI circuits [5]. There are three performance parameters on which a VLSI designer has to optimize their design i.e. Area, Speed and Power [10]. The design of faster, smaller and more efficient adder architecture has been the focus of many research efforts [8].

CLA are very important building block for any digital circuits. In this paper, the CLA has been implemented using different static and dynamic logic style like standard CMOS, Differential Cascode Voltage Switch (DCVS) logic, Pseudo NMOS logic, Pass Transistor Logic (PTL) and Domino logic. Tanner simulation results has been done for different feature size of 150nm, 200nm and 250nm to determine the propagation delay, average power consumption and their Power delay product (PDP). The performance of CLA has been observed by considering both intrinsic and extrinsic load capacitance.

The rest of paper is organized as follows. Section II describes the block diagram and its basic construction of CLA. The details design of CLA using different logic style has been given in section III. Different performance parameters are discussed in section IV. Section V gives the complete simulation results and their discussion. The paper is concluded in section VI.

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II. DESIGN OF CARRY LOOK AHEAD ADDER

In this section, the basic design structure has been discussed. The carry look-ahead logic uses the concepts of generating and propagating the carry bit. Although in the context of a carry look-ahead adder, it is most natural to think of generating and propagating in the context of binary addition [1-3]. The table1 showing the addition of two 8bit binary no in the CLA. Initial carry C_0 is logic0 and after addition the final carry will be logic1. The final carry will not depends on intermediate carry depends only on input bits.

Table No: 1 – Addition of two 8bit binary numbers in CLA Adder

					$C_0 = 0$				
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	= 255
	1	1	1	1	1	1	1	1	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	= 255
	1	1	1	1	1	1	1	1	
1	1	1	1	1	1	1	1	1	= 511
C_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	

The 8-bit CLA adder can be built by using 8bit full adder (FA) and the Carry Look-ahead logic block as shown in fig1.

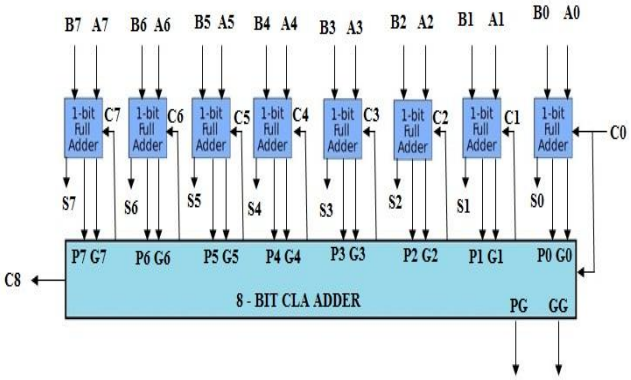

Fig1: Block diagram of 8bit Carry Look-Ahead Adder

The expression for Carry propagate, $P_i = A_i \oplus B_i$

Carry generate, $G_i = A_i.B_i$, sum expression,

$S_i = P_i \oplus C_i$ and Carry out $C_{i+1} = G_i + P_i C_i$

Signals P and G only depend on the input bits

$C_1 = G0 + P_0.C_0$

$C_2 = G1 + P_1.C_1 = G_1 + P_1.G_0 + P_1.P_0.C_0$

$C_3 = G_2 + P_2.G_1 + P_2.P_1.G_0 + P_2.P_1.P_0.C_0$

$C_4 = G_3 + P_3.G_2 + P_3.P_2.G_1 + P_3P_2.P_1.G_0 + P_3P_2.P_1.P_0.C_0$

$C_5 = G_4 + P_4G_3 + P_4P_3G_2 + P_4P_3P_2G_1 + P_4P_3P_2P_1G_0 + P_4P_3P_2P_1P_0C_0$

$C_6 = G_5 + P_5G_4 + P_5P_4G_3 + P_5P_4P_3G_2 + P_5P_4P_3P_2G_1 + P_5P_4P_3P_2P_1G_0 + P_5P_4P_3P_2P_1P_0C_0$

$C_7 = G_6 + P_6G_5 + P_6P_5G_4 + P_6P_5P_4G_3 + P_6P_5P_4P_3G_2 + P_6P_5P_4P_3P_2G_1 + P_6P_5P_4P_3P_2P_1G_0 + P_6P_5P_4P_3P_2P_1P_0C_0$

$C_8 = G_7 + P_7G_6 + P_7P_6G_5 + P_7P_6P_5G_4 + P_7P_6P_5P_4G_3 + P_7P_6P_5P_4P_3G_2 + P_7P_6P_5P_4P_3P_2G_1 + P_7P_6P_5P_4P_3P_2P_1G_0 + P_7P_6P_5P_4P_3P_2P_1P_0C_0$

Fig2 giving the gate level architecture of 4bit carry look-ahead adder.

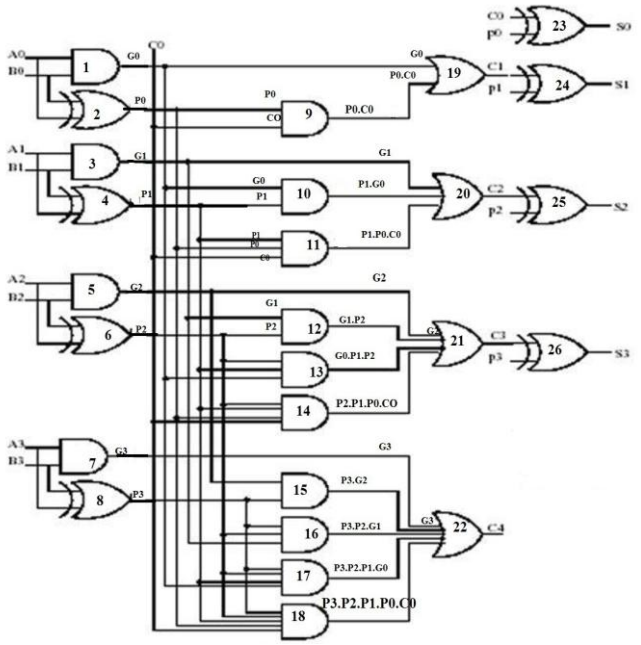

Fig2: Gate level architecture of 4bit Carry Look-Ahead Adder

The input and output waveforms of CLA are showing in the fig3.

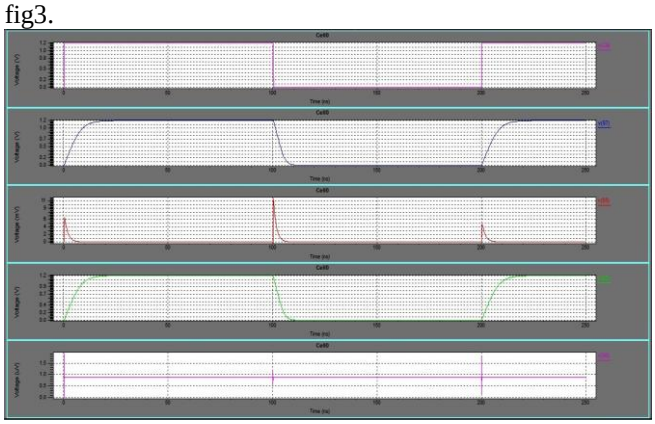

Fig3: Output waveform of Carry Look-Ahead Adder

In the following section different types of static logic CLA circuits are described.

III. DIFFERENT DESIGN STYLES

Here the standard CMOS logic, DCVS logic, Pseudo NMOS and Domino logic are given and by using this logic style the CLA has been implemented.

a) *Standard Cmos Logic*

The most widely used logic style is standard CMOS. The fig3 shows a generic N input logic gate where all inputs are distributed to both the pull-up and pull-down networks. The PDN is constructed using NMOS devices, while pMOS transistors are used in the PUN [9,11]

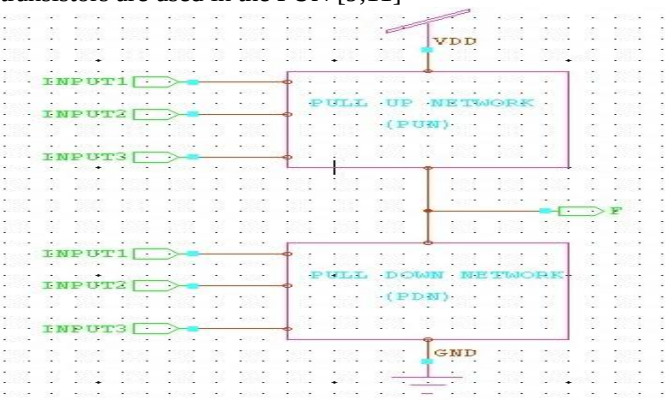

Fig4: Block diagram of Standard CMOS logic

Some of the positive side of this standard CMOS are 1) Outputs are well defined. 2) Output voltage is not changing with time. 3) Periodic signals or clocks are not required for refreshing the voltage of nodes. 4) Robust structure (i.e., low sensitivity to noise and 5) Low power consumption with no static power dissipation in ideal situation. And some negative points are 1) The number of transistors required to implement an N fan-in gate is 2N, hence large area. and 2) The propagation delay of a complementary CMOS gate deteriorates rapidly as a function of the fan-in

b) Differential Cascode Voltage Switch Logic (Dcvsl)

The DCVSL gate provides differential (or complementary) outputs [4]. Both the output signal (out) and its inverted value (inverted out) are simultaneously available. It has been observed that a differential implementation of a complex function may reduce the number of gates required by a factor of two. The number of gates in the critical timing path is often reduced as well.

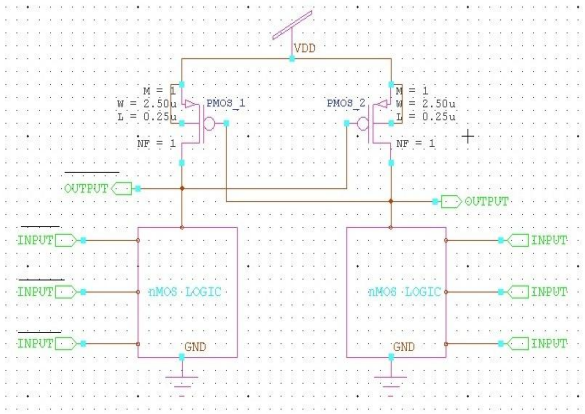

Fig5: Block diagram of Standard DCVS logic

The advantages of DCVS logic are 1) Both true and complement form of inputs and outputs are used, as a result no extra inverter circuit required. 2) Ideally zero static power dissipation. 3) High speed and 4) Reduced input capacitance. Some drawback this logic are 1) More interconnection required and 2) High dynamic power dissipation

c) Pseudo Nmos Logic

Pseudo NMOS logic design is one way to reduce the transistor count [8-9]. Pull up network (PUN) is grounded, so it is always ON. The main reason to reduce this width is to improve the noise margin & speed. Purpose of PUN is to provide a conditional path between V_{DD} and the output when pull down network (PDN) is OFF. Pseudo NMOS logic is also known as ratioed logic. The main advantages of Pseudo NMOS logic are higher packing density and less chip area.

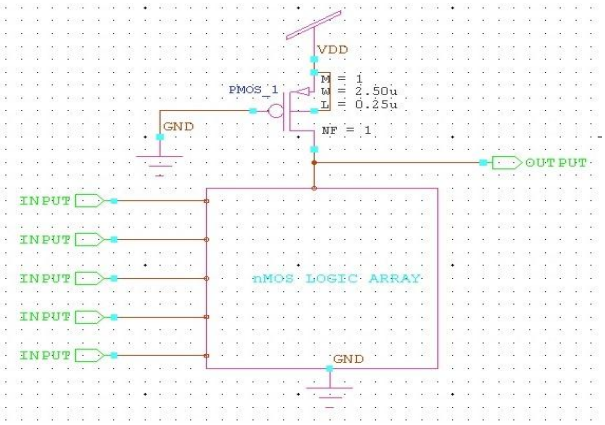

Fig6: Block diagram of Pseudo NMOS logic

It has also some drawbacks – static power dissipation is one of them. In Pseudo NMOS under low condition a steady state DC current will flow in the p-Channel load & PDN, as a result static power dissipation is occurred.

d) Pass-Transistor Logic (Ptl)

A popular and widely-used alternative to complementary CMOS is pass-transistor logic, which attempts to reduce the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source/drain terminals.

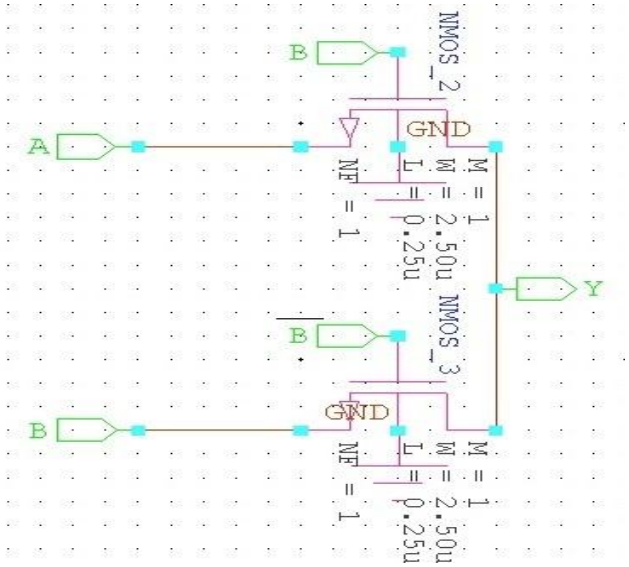

Fig:7 Bock Diagram of Pass Transistor Logic

Figure7 shows an implementation of the AND function constructed that way, using only NMOS transistors. Its presence is essential to ensure that the gate is static; this is that a low-impedance path exists to the supply rails under all circumstances, or, in this particular case, when B is low. The promise of this approach is that fewer transistors are required to implement a given function. The reduced number of devices has the additional advantage of lower capacitance. The advantages of this logic are 1) Both the gate & source/drain terminals are used as input port. 2) Number of transistor is lesser than Standard CMOS design and 3) Well suited for implementation of 6 transistor RAM, Full adder, XOR gate. The drawbacks of this logic are 1) PTL suffers from limited output swing, 2) Static power dissipation & 3) Low noise immunity.

e) Domino Logic

A Domino logic module consists of an n-type dynamic logic block followed by a static inverter .During pre-charge, the output of the n-type dynamic gate is charged up to V_{DD}, and the output of the inverter is set to 0. During evaluation, the dynamic gate conditionally discharges, and the output of the inverter makes a conditional transition from 0 to 1. If one assumes that all the inputs of a Domino gate are outputs of other Domino gates, then it is ensured that all inputs are set to 0 at the end of the pre-charge phase, and that the only transitions during evaluation are 0 to 1 transitions. The formulated rule is hence obeyed. The introduction of the static inverter has the additional advantage that the fan-out of the gate is driven by a static inverter with a low impedance output, which increases noise immunity. The buffer furthermore reduces the capacitance of the dynamic output node by separating internal and load capacitances. Consider now the operation of a chain of Domino gates. During pre-charge, all inputs are set to 0. During evaluation, the output of the first Domino block either stays at 0 or makes a 0 to 1 transition, affecting the second gate.

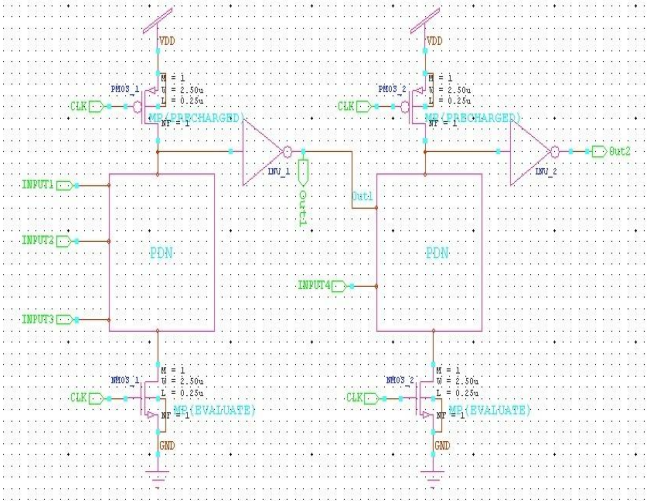

Fig 8: Bock Diagram of Domino Logic

Since each dynamic gate has a static inverter, only non-inverting logic can be implemented. Although there are ways to deal with this, as is discussed in a subsequent section, this is major limiting factor, and pure Domino design has become rare. Very high speeds can be achieved: only a rising edge delay exists, while t_{pHL} equals zero. The inverter can be sized to match the fan-out, which is already much smaller than in the complimentary static CMOS case, as only a single gate capacitance has to be accounted for per fan-out gate.

The advantages of Domino logic are 1) Since PMOS transistors are eliminated, the output capacitance is smaller leading to higher speed during switching time, 2) Dynamic

logic typically takes smaller area than the equivalent static circuits. 3) No of transistor = n+4 transistors. Drawbacks are 1) Charge sharing, 2) Charge leakage, 3) Can have static power dissipation, 4) More complex control (generate pre-charge signal , 5) Logic clocking can substantially increase power consumption and may consume 20% of the total chip power and 6) Dynamic nodes are kept floating at the evaluation time and this makes them vulnerable to noise, leakage and failure mechanisms.

IV. PERFORMANECE PARAMETERS OF CLA

a) Power dissipation

Power dissipation is a measure of the power consumed by the logic gate when fully driven by all its input. The D.C or average power dissipation is the product of D.C supply voltage and the mean current taken from the supply. Ideally, CMOS circuits dissipate no static (DC) power, since in the steady state there is no direct path from VDD to ground. There are always leakage currents and substrate injection currents which leads to static power dissipation in CMOS circuits .One of the dynamic components of power dissipation arises from the transient switching behavior of the CMOS devices. At some point during the switching transient, both the NMOS and PMOS devices are on and a short circuit current exists between VDD and ground. Another component of dynamic power dissipation is charging and discharging of parasitic capacitances which consume most of the power used in CMOS circuits. This leads to the conclusion that CMOS power consumption depends on the switching activity of the signals involved. If we show the switching activity by a parameter α, then we can compute the whole power dissipation through the following equation-

$$P = \alpha C_L V^2_{DD} f_{clk} + (I_{sc} + I_{Leakage})\, V_{DD}$$

Where, f is the clock frequency of logic operation, C_L is the total capacitance (parasitic capacitance, fault capacitance, interconnect capacitance) charged and discharged every cycle and V_{DD} is the power supply voltage. I_{sc} and $I_{leakage}$ are the short circuit current and leakage current respectively. As we see in the above formula, power supply voltage has a quadratic relationship with the power; therefore voltage reduction offers the most dramatic means of minimizing energy consumption.

b) Propagation Delay:

The propagation delay, can be defined as time required to reach $0.5V_{DD}$ of output from the $0.5V_{DD}$ of input. The propagation delays of CLA are measured in the order of nano second.

c) *Power Delay Product*

Power Delay Product is the product of average power dissipation to the propagation delay ((PDP=average power consumed * propagation delay), in fJ ($10^{\wedge -15}$)).

V. SIMULATION RESULTS & DICUSSIONS

All the simulation results are observed from Tanner simulation tool version 13.1. Comparisons of 4bit & 8bit CLA are done by varying different channel length and different load capacitance. Power dissipation, Propagation delay of sum and final carry and their corresponding PDP are measured in this work.

Fig9 shows the average power consumption of standard CMOS, DCVS & Pseudo NMOS CLA for different feature size. Maximum and minimum average power is found in Pseudo NMOS CLA and standard CMOS CLA respectively.

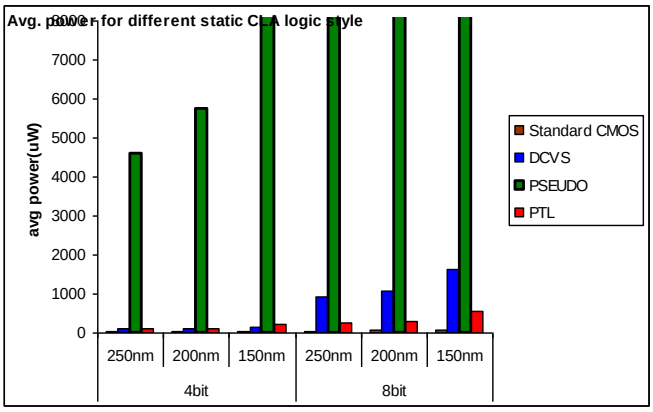

Fig9: Average power consumption of 4bit and 8bit CLA for different channel lengths (L=250nm,200nm, 150nm)

Fig10 shows the final carry propagation delay of standard CMOS, DCVS & Pseudo NMOS CLA for different channel length. Maximum and minimum carry propagation delay is found in DCVS CLA and Pseudo NMOS CLA respectively.

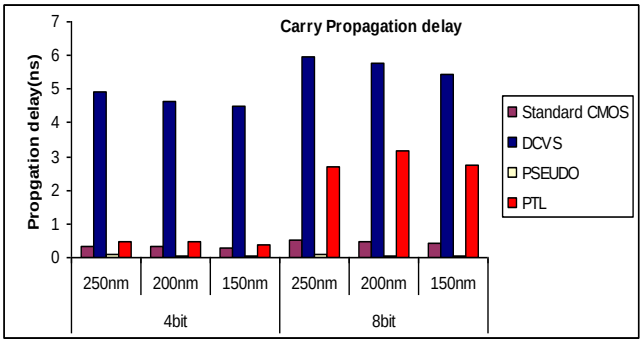

Fig10: Propagation delay of final carry output of 4bit and 8bit CLA for different channel lengths (L=250nm,200nm, 150nm)

Fig11 note the sum propagation delay of standard CMOS, DCVS & Pseudo NMOS CLA for different feature size. Maximum and minimum sum propagation delay is found in PTL CLA and Pseudo NMOS CLA respectively.

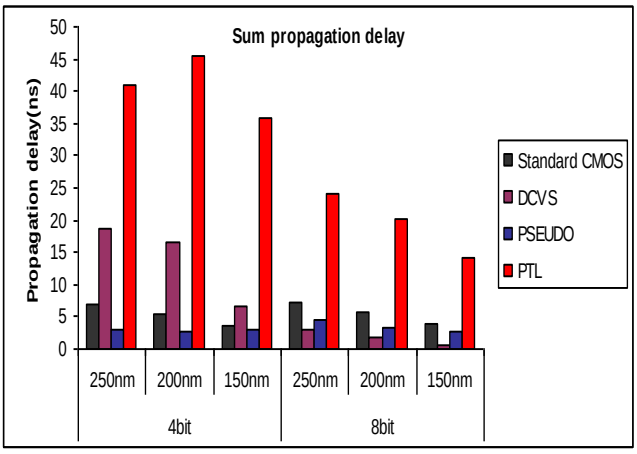

Fig11: Propagation delay of sum output of 4bit and 8bit CLA for different channel lengths (L=250nm,200nm, 150nm)

Fig12 note the PDP of final carry of standard CMOS, DCVS & Pseudo NMOS CLA for different feature size. Maximum and minimum PDP of final carry is found in DCVS CLA and standard CMOS CLA respectively.

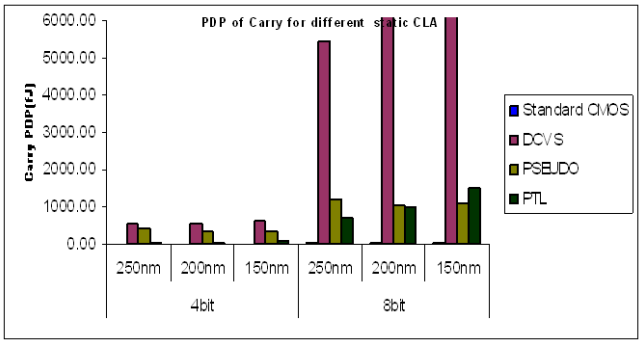

Fig12: Power Delay Product (PDP) of 4bit and 8bit CLA for different channel lengths (L=250nm,200nm, 150nm)

Fig13 note the PDP of sum of standard CMOS, DCVS & Pseudo NMOS CLA for different feature size. Maximum and minimum PDP of sum is found in Pseudo NMOS CLA and standard CMOS CLA respectively.

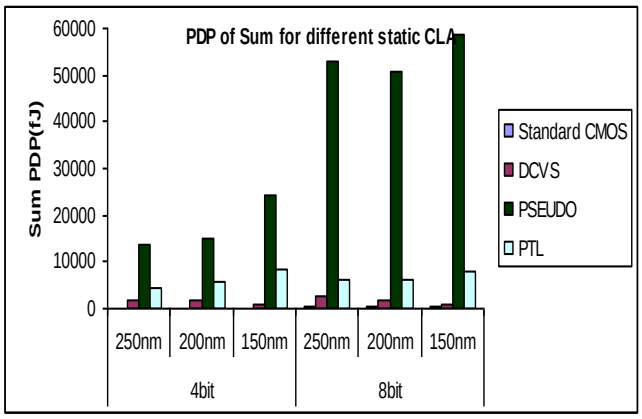

Fig13: Power Delay Product (PDP) of 4bit and 8bit CLA for different channel lengths (L=250nm,200nm, 150nm)

Fig14 shows the no of transistors required to implement 4bit and 8bit CLA. Highest no of transistors are required in DCVS CLA and Lowest no of transistors are required in Pseudo NMOS CLA.

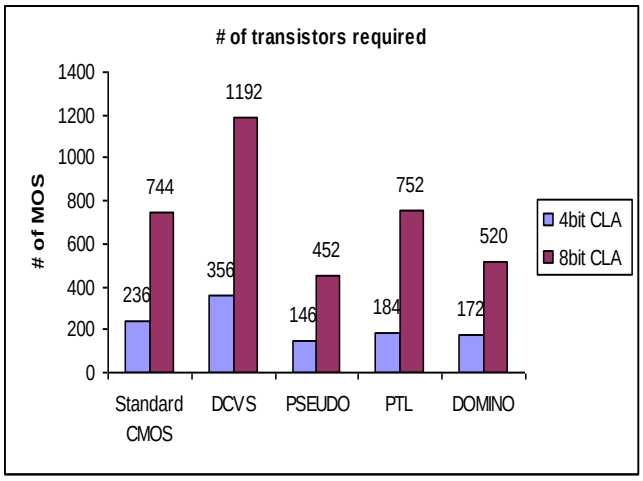

Fig14: # Transistors required to implement 4bit and 8bit CLA

Table2 & Table3 are showing the details simulation results of different static & dynamic logic styles implementation of CLA using both external capacitace (100fF) and without external capacitances.

Table No: 2 Simulation results of different static & dynamic logic style CLA by considering an external load capacitor (100fF)

LOGIC STYLE		INPUT BIT	NO OF TRANSISTOR	CHANNEL LENGTH (nm)	AVG POWER CONSUMED (uW)	PROPAGATION DELAY (ns)		PDP (fJ)	
						CARRY	SUM	CARRY	SUM
STATIC LOGIC	STANDARD CMOS CLA	4	236	250	**20.75**	0.34	6.93	**7.06**	143.8
				200	25.46	0.31	5.48	7.89	139.52
				150	30.25	0.28	3.74	8.47	**113.14**
		8	744	250	52.64	0.51	7.24	26.85	381.11
				200	61.85	0.46	5.69	28.45	351.93
				150	66.28	0.42	3.87	27.84	256.5
	DCVS CLA	4	356	250	106.04	4.93	18.67	522.78	1979.77
				200	116.65	4.64	16.57	541.26	1932.89
				150	140.28	4.51	6.49	632.66	910.42
		8	1192	250	914.9	5.98	3.01	5471.1	2753.85
				200	1075.18	5.76	1.66	6193.04	1784.8
				150	1622.43	5.46	0.52	8858.47	843.66
	PSEUDO nMOS CLA	4	146	250	4589.3	0.09	2.99	413.04	13722.01
				200	5757.78	0.06	2.63	345.47	15142.96
				150	8317.39	0.04	2.94	332.7	24453.13
		8	452	250	11885.59	0.1	4.44	1188.56	52772.02

				200	14923.1	0.07	3.4	1044.62	50738.54
				150	***21529.99***	0.05	2.73	1076.5	***58776.87***
	PASS TRANSISTOR LOGIC (PTL)	4	184	250	109.92	0.49	41.08	53.41	4515.95
				200	128.24	0.45	45.36	57.6	5816.25
				150	236.57	0.38	35.97	89.73	8510.15
		8	752	250	263.08	2.69	24.02	707.11	6317.89
				200	308.87	3.18	20.29	981.54	6267.98
				150	553.12	2.73	14.29	1510.4	7902.95
DYNAMIC LOGIC	**DOMINO**	4	172	250	*112.49*	0.12	3.82	13.4	429.53
				200	134.15	0.09	3.08	12.26	*413.76*
				150	180.16	*0.05*	*2.21*	*9.57*	398.66
		8	520	250	142.6	0.13	3.83	18.53	546.3
				200	164.07	0.1	3.09	16.14	506.46
				150	210.01	0.06	2.22	12.59	465.24

Table No: 3 Simulation results of different logic style implementation of CLA for intrinsic load capacitor

LOGIC STYLE		**INPUT BIT**	**CHANNEL LENGTH (nm)**	**AVG POWER CONSUMED (uW)**	**PROPAGATION DELAY(ns)**		**PDP(fJ)**	
					CARRY	**SUM**	**CARRY**	**SUM**
STATIC LOGIC	**STANDARD CMOS CLA**	4	250	**1.94**	0.31	2.37	0.6	4.6
			200	2.67	0.27	1.25	0.72	**3.34**
			150	3.18	0.21	1.13	0.67	3.59
		8	250	4.03	0.51	2.68	2.06	10.8
			200	4.25	0.46	2.47	1.96	10.5
			150	4.72	0.41	2.26	1.94	10.67
	DCVS CLA	4	250	46.06	3.99	9.68	183.78	445.86
			200	55.37	3.52	9.08	194.9	502.76
			150	65.27	1.14	6.67	74.41	435.35
		8	250	817.33	5.34	10.94	***4364.54***	8941.59
			200	1033.64	2.65	11.62	2739.15	12010.9
			150	***1512.43***	1.5	12.5	2268.65	*18905.38*
	PSEUDO nMOS CLA	4	250	4488.85	0.08	1.32	359.11	5925.28
			200	5657.31	0.05	1.12	282.87	6336.19
			150	8216.97	0.03	1.01	246.51	8299.14
		8	250	11784.69	0.08	1.14	942.78	13434.55
			200	14722.17	0.06	1.11	883.33	16341.61
			150	21429.18	0.05	1.07	1071.46	22929.22
	PASS TRANSISTOR LOGIC (PTL)	4	250	97.49	1.94	3.65	189.04	356.31
			200	116.15	2.45	4.52	284.68	525.24
			150	207.69	2.53	4.08	526.14	848.04
		8	250	116.19	2.68	0.49	310.81	56.46
			200	142.1	3.16	0.36	448.76	50.61
			150	483.68	2.7	0.21	1307.1	103.84
DYNAMIC LOGIC	**DOMINO**	4	250	84.08	0.12	0.17	10.45	14.54
			200	105.79	0.09	0.12	9.58	13.12
			150	151.7	0.05	0.08	7.97	11.79
		8	250	85.4	0.13	0.19	11.49	15.83
			200	106.93	0.1	0.13	10.36	14.19
			150	152.73	0.06	0.08	9.1	12.78

VI. CONCLUSION

Comparative performance analysis of different static and dynamic CLA has been carried out by this work. Different graphs are showing that by varying the channel length how performance of the CLA has been changed. Average power and PDP for sum & carry are found minimum in case 4bit standard CMOS CLA implementation. Average power and PDP for sum & carry are found maximum in case 8bit Pseudo NMOS CLA implementation. This work will helpful for designer to implement any type of digital VLSI adder circuits.

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