InGaAs/GaAs HEMT for High Frequency Applications

N V Uma Reddy, M V Chaitanya Kumar

Abstract -In the modern VLSI especially for high speed devices, where the conventional MOSFET technology is reaching its limitations due to various short channel effects and velocity saturation effects etc, hetero-junction FETs have shown great promise for high speed devices. Novel HEMT device using heterojunctions made of $InGaAs$ and $InAlAs$ on a $GaAs$ substrate is designed and modeled using TCAD software. Highly doped deep source-drain implants are proposed for the design. The device simulations have demonstrated its utility towards high frequency applications in GHz range.

Keywords- HEMT, $InGaAs$, $InAlAs$

I. INTRODUCTION

Recent developments in satellite communications and broadband communications have led the microelectronics industry to develop and fabricate devices with increasing cut-off frequency. Heterojunction bipolar transistors show good cut-off frequencies but are poor in noise performance [1]. Unipolar devices, mainly high-electron mobility transistors (HEMTs) provide high frequency performance at low noise levels. This property is the result of the higher electron mobilities of the materials involved, higher saturation velocities and higher electron densities [2].

Improvements in device performance can be obtained by reducing the gate length. However, short channel effects limit the microwave performance of the device due to which, the tradeoff between the layer structure and the device geometry should be optimally designed using computer simulations, to help reduce time and cost [2].

Indium content in the devices provides them an improved RF performance, but higher Indium content leads to lower breakdown, kink effect. Parasitic source to drain(S/D) resistance also degrades the high frequency performance of the device. Hence a lower S/D resistance is desirable [3].

In this paper, a novel $InAlAs$ channel HEMT with source drain regions of highly doped $InGaAs$ is presented. Induced strain in the channel is utilized for mobility improvement. Higher S/D doping concentration reduces the series source-drain resistance.

Manuscript received on March, 2013

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II. HETEROJUNCTIONS

Hetero-junctions refer to the interface between two layers of dissimilar crystalline semiconductors [2], where the conventional MOSFET technology is reaching its limitations due to various short channel effects and velocity saturation effects etc, hetero-junction FETs have shown great promise for high speed devices. In contrast to the homo-junctions, hetero-junctions have materials with unequal band gaps (mostly $III-V$ semiconductors) and the device properties depend on the mismatch in the band gap of the materials. The band gap in the $III-V$ semiconductors can be engineered by varying the mole fraction of the constituents and hence the devices properties can also be tailored. A typical band diagram of a hetero-junction is shown in Figure 1.

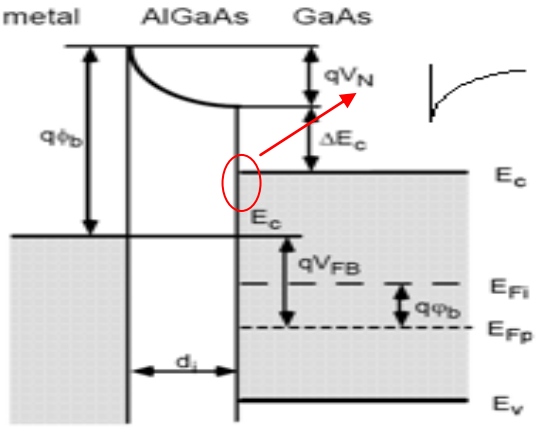

Figure 1 Band Diagram in Hetero-Junctions (where notations have their usual meanings)

Hetero-junctions achieve high mobility and high electron concentration by concentrating the carriers into a region devoid of any ions. Hence the mobility degradation due to the ionized ion scattering is absent.

The idea behind making a hetero-junction FET is to have a high band gap material followed by a low band gap material so as to form a potential well(quantum well) (the notch as visible in the above figure). In conventional MOSFETs, the channel or a quantum well is formed at the interface between oxide (high band-gap) and bulk silicon (low band-gap).

For a given doping level, as a result of discontinuity in the conduction band, band bending is more in the Heterojunction than in the homojunction. The larger band bending will result in the edge of conduction band in the neutral region being raised by ΔE_c. ΔE_cdetermines electron concentration in the quantum well. Further, Φ_s, the potential barrier is higher in the Heterojunction than the homojunction by $\Delta E_c/q$.

$$\Phi_s(\text{hetro}) = \Phi_s(\text{homo}) + \Delta E_c/q$$

III. DEVICE SIMULATION

Figure 2 shows the device structure for the simulated HEMT structure. $In_x\ Al_{(1-x)}\ As$ layer forms the active channel region and is separated from the $GaAs$ substrate by $In_x\ Al_{(1-x)}\ As$. The device structure for simulation is obtained by simulating the fabrication steps as mentioned in the following section.

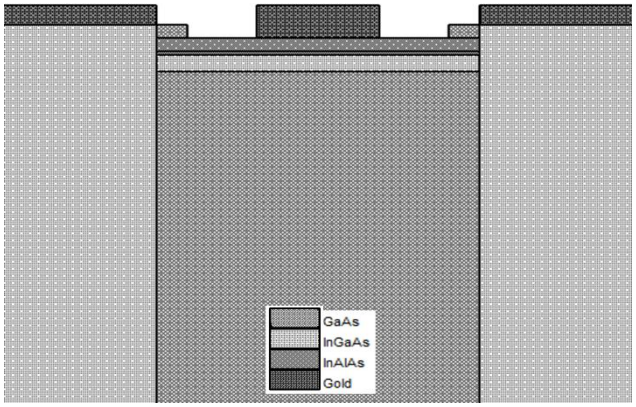

Figure 2 HEMT Structure

$In_x\ Al_{(1-x)}\ As$) and $In_x\ Al_{(1-x)}\ As$ are grown on $GaAs$ substrate using molecular beam epitaxy (MBE) process.where $x = 0.48$. Wet chemical MESA etching is used to isolate the active area of the device. Deep source and drain regions are realized with highly doped $In_{0.6}Ga_{0.4}As$. To obtain source-drain contacts, gold is evaporated and then alloyed at $250°C$ using rapid thermal annealing. Gate metal contacts are deposited as Schottky gate metal using Gold lift-off. The device is passivated using Si_3N_4 deposited by plasma enhanced chemical vapor deposition.

IV. ANALYTICAL DESCRIPTION OF OPERATION

A. Analytical expression for 2DEG (two dimensional elecctron gas) density:

The basic qualitatively description of HEMT's operation is based on 1-dimensional charge control model at the direction perpendicular to the hetero-interface. The electric potential (band diagram) and charge distribution follows the Poisson's equation and the electron wave function satisfy the Schrodinger's equation [4]. Theoretically the potential and charge profile can be calculated by self-consistently solving the two equations. Based on the assumption that the charge depleted from the donor layer is accumulated in the 2DEG, the Fermi level is constant across hetero-interface, and the interfacial potential at the channel can be approximated by a triangular well, the electron charge(n_s) stored at the interface in a modulation doped structure is [5]

$$n_s = \frac{\in}{q_d}\left[V_g - \left(\Phi_B - V_p + {}^{E_{fi}}/_{q} - {}^{\Delta E_c}/_{q}\right)\right] \qquad \ldots(2)$$

where ∈ is the dielectric constant of the barrier layer, q is electron static charge, d is sum of the thickness of undoped barrier d_i and doped barrier d_d, V_g is the applied gate to source voltage, $\Phi_B$is the Schottky barrier height of the gate metal deposited on the barrier layer, $V_p = \frac{qN_d d_d^2}{2\in}$ while N_d is the donor concentration in the barrier layer, E_{fi} is the Fermi level with respect to the conduction band edge in the channel layer, and ΔE_c is the conduction band offset between the barrier and channel [5].

The threshold voltage is given as [6]:

$$V_{th} = \Phi_B - \frac{\Delta E_c}{q} - V_p + \frac{E_{fi}}{q} \qquad \ldots(3)$$

for modulation doped structure.

Transconductance, $g_m$is defined as the change in the drain to source current divided by the change in the gate to source voltage at certain drain to source voltage [2]

$$g_m = \frac{dI_d}{dV_g}|V_{ds=\ Constant} \qquad \ldots(4)$$

It is the most important dc figure of merit in field effect transistors as it demonstrates the current modulation efficiency of the gate.

V_t was computed to be $-0.727V$ for the proposed HEMT structure.

V. DEVICE MODELING

The HEMT device structure was modeled in TCAD software. Figure 3 shows the HEMT structure built using TCAD tool. After building the structure and assigning the material properties, device simulations were carried out.

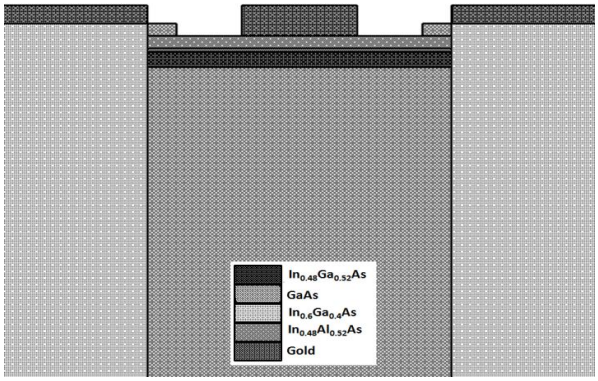

Figure 3 HEMT structure modeled in SILVACO

Doping concentrations were extracted across different sections along the device. The doping profiles are summarized in figure 5 to 8.

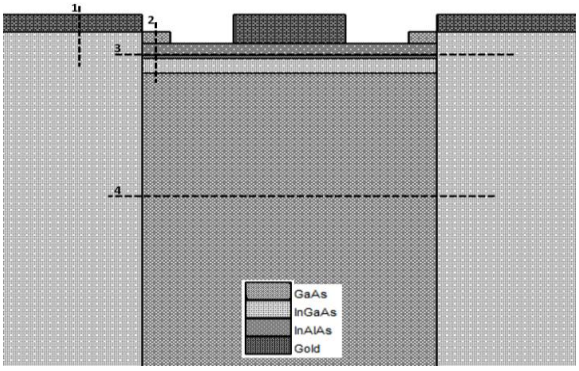

Figure 4 Cut Sections

Doping concentration contours near the junctions are extracted from the simulation and presented in figure 9.

HEMT performance was simulated using TCAD and device was characterized through its $Id-Vds$, $Id-Vgs$ current gain plots. Device transconductance, threshold voltage, unity gain frequency were extracted from the simulation results. Different results are presented in Section VI.

VI. RESULTS AND DISCUSSION

- Doping concentrations in the device across various cross-sections are shown in Figures 5 to 8. The cross sections are defined as in Figure 4. Figure 5 shows the doping concentration is high in the $InGaAs$ S/D regions. Figure 6 depicts the doping profile along section 2. It depicts the presence of a relatively high doped $In\,Al\,As$ layer. Figure 7 demonstrates highly doped source/ drain regions with lightly doped channel layer. The simulation results confirm the high doping levels in the $InGaAs$ deep source drains to the order of 10^{19-20}. Figure 8 shows the doping profiles for the deep S/D and the substrates. The doping profile of S/D is of the order of 10^{19-20}whereas the $GaAs$ substrate is intrinsic at higher depths.
- Band structure was extracted for the HEMT device and is shown in Figure 10. The presence of a quantum well type of structure can be observed. The figure shows the band offsets in the conduction band and the valence band between the $InAlAs-InGaAs-GaAs$ Heterojunction. These band offsets give rise to the band bending and hence the confinement of the charge carriers.
- Total current density is plotted in Figure 11. The maximum current density is observed in the $InGaAs$ layer as expected and is around $16e5\ A/cm^2$.
- Threshold voltage of the device can be obtained from the slope of the $Id-Vg$ plot. From figure 12, the max slope of the plot occurs at $-0.4V$. Hence the approximate threshold voltage for the device from the simulations is around $-0.4V$ which is near to the calculated value of $-0.727V$.
- The $Id-Vds$ plot in Figure 13 shows a nearly flat region at $Vds = 0.5V$ and above. The device is operating in the saturation in this region. The drain current practically is not changing in this region as a result of the Vds bias and hence is fully controlled by the gate voltage only.
- Figure 14 shows the gate capacitance variation with the gate bias. It shows a typical curve like that of a MOSFET device with device operating in accumulation for $Vgs > 1V$ and in inversion region for $Vgs < 0V$. The steep transition from accumulation to inversion or vice-versa shows that there are very few trapped impurities in the device.
- The AC analysis shows that the current gain is flat up to $10\ kHz$ and has a unity gain frequency beyond $100GHz$ and hence is usable for high frequency applications. High current gain of $160dB$ and transconductance gain of $90dB$ is obtained for the device.

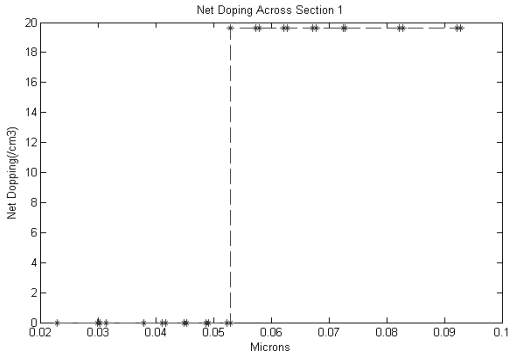

Figure 5 Net Doping across Section1

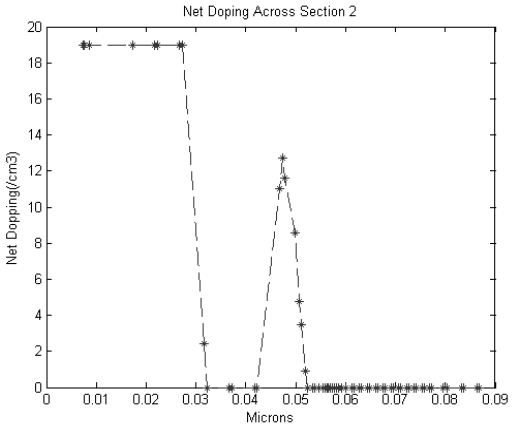

Figure 6 Net Doping across Section 2

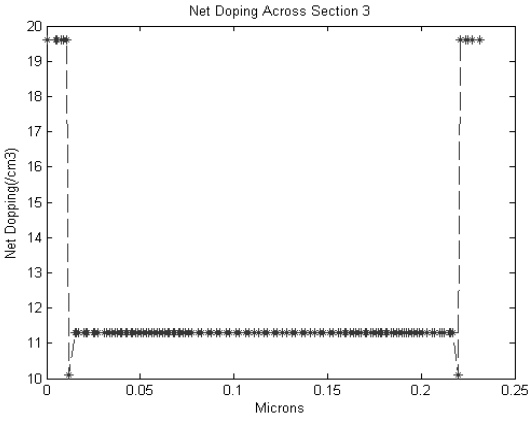

Figure 7 Net Doping across Section 3

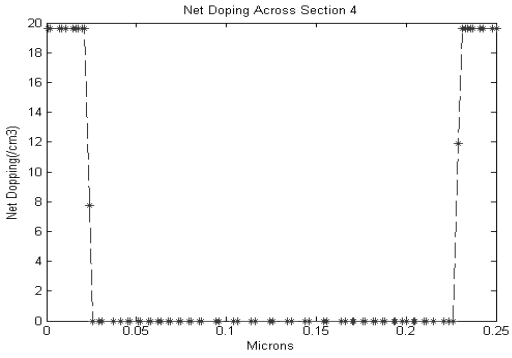

Figure 8 Net Doping across Section 4

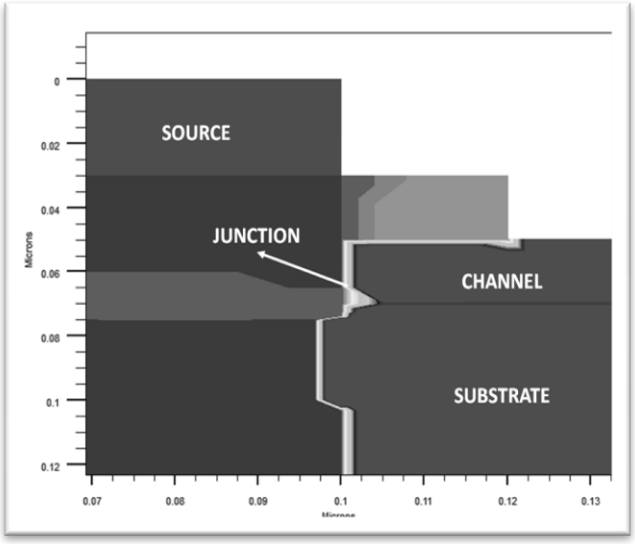

Figure 9 Depletion layers at Junctions

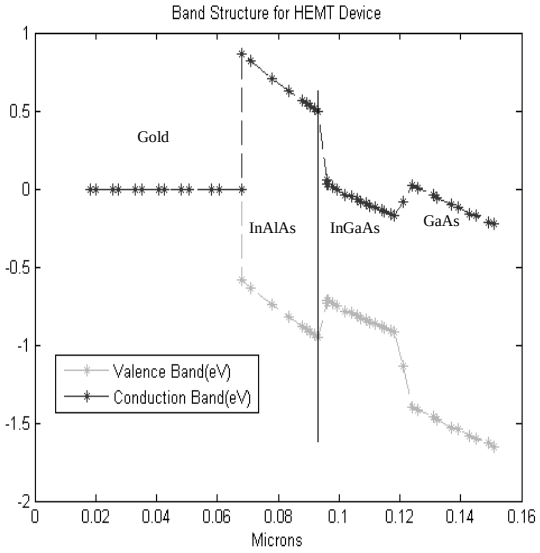

Figure 10 Band structure for the HEMT device

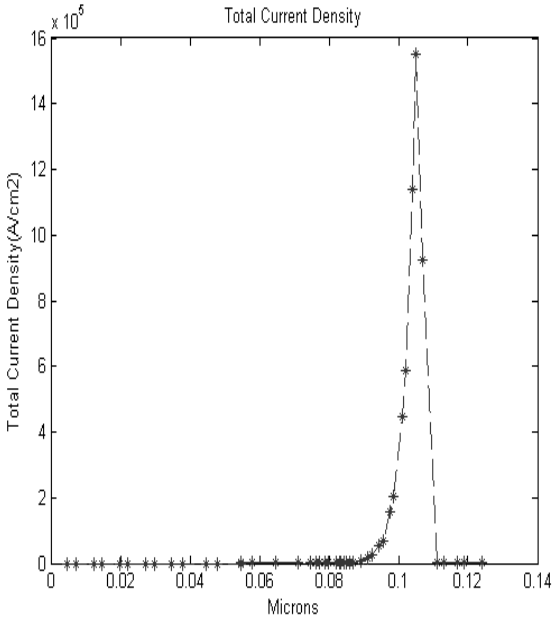

Figure 11Total Current Density

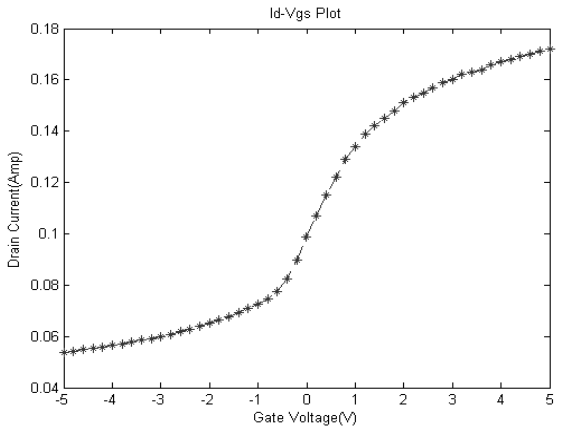

Figure 12 I_d-V_{gs} plot

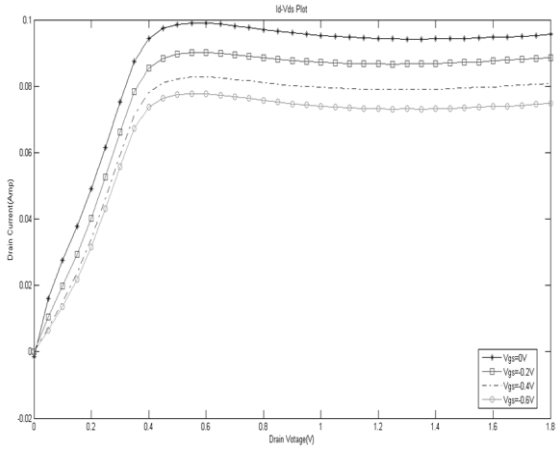

Figure 13 I_d-V_{ds} plot

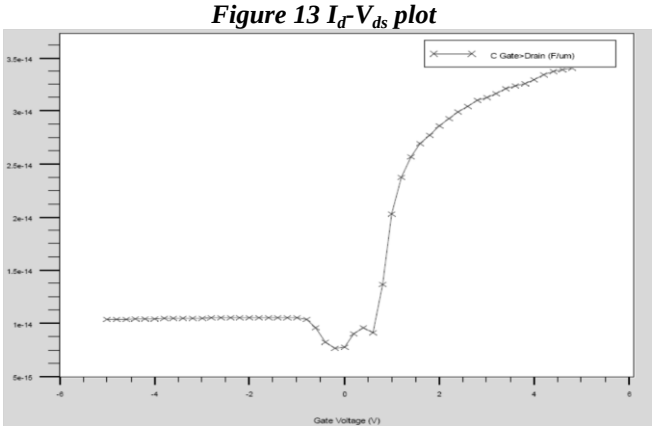

Figure 14 Gate Capacitances (V_{ds}=0.5V)

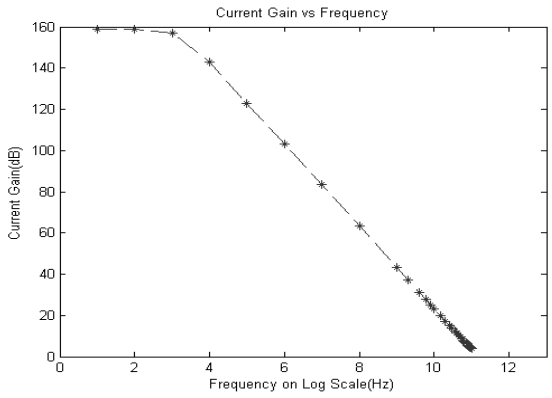

Figure 15Current gain v/s Frequency

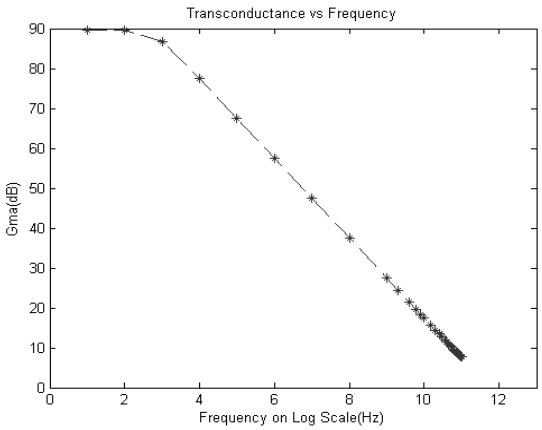

Figure 16 Trans-conductance v/s frequency

VII. CONCLUSION

A Heterojunction HEMT is designed and modeled using TCAD software and the device performance is simulated. The device shows high unity gain bandwidth of the order of $100GHz$ which makes the device promising for use in high frequency applications. The device shows good output impedance as is evident from the $Id - Vgs$ plot. The device has shown a current gain of 140 dB and a trans-conductance gain of 75 dB.

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