High Performance Optimization of Low Power Multi -Threshold Voltage using Level Converters

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Abstract— Applying multiple supply voltages (multi- VDD) is an effective technique for reducing the power consumption without reducing speed in an integrated circuit (IC). In order to transfer signals among the circuits operating at different supply voltages specialized voltage level converters are required. Two new multi threshold voltage (multi-V_{TH}) level converters are proposed in this paper. The proposed level converters are compared with the level converters in [7], for operation at different supply voltages. When the level converters are individually optimized for minimum power consumption and propagation delay, the proposed level converters offers significant power saving and speed is enhanced as compared to the level converter in [7] of same technology.

Index Terms— High-performance, multiple supply voltages, multiple threshold voltages, power efficiency, voltage level converters

I. INTRODUCTION

Technology scaling is the main thrust behind the advancement of CMOS technology. More and faster transistors are crammed onto integrated circuits with each new technology generation. The increased number of transistors and the enhanced clock frequency lead to a significant increase in the power consumption with each new technology generation. Furthermore, deviation from the constant field scaling due to the non-scaling parameters of the MOS transistors (the thermal voltage, the silicon energy band gap, and the source/drain doping levels) leads to an increase in the power density. The higher power dissipation coupled with the imbalanced utilization and the diversity of circuitry elevates the temperature and produces local hot-spots across a die [1]. The increased power dissipation degrades the reliability, increases the cost of the packaging and cooling system, and lowers the battery lifetime in portable electronic devices.

An effective method for reducing the power consumption is scaling the supply voltage. Dynamic, short-circuit, and leakage components of power consumption are simultaneously reduced with the scaling of the supply voltage in a CMOS circuit. Lowering the supply voltage, however, also degrades signal propagation paths the circuits speed. The multi-VDD circuit technique exploits the delay differences among the different within an integrated circuit (IC) [1].The supply voltages of the gates on the noncritical delay paths are selectively lowered while a higher supply Voltage is maintained on the critical delay paths in order to satisfy a target clock frequency in a (multi-VDD) circuit.

Similarly, in systems-on-chips (SOCs), different circuits operating at different supply voltages exist .When a low voltage swing signal drives a CMOS gate connected to a higher supply voltage, static dc power is consumed as the transistors in the pull-up and the pull-down networks are simultaneously turned on [1]. Furthermore, the output voltage swing of the receiver degrades, thereby leading to a static dc current in the fan-out gates of the receiver. In order to transfer signals among these circuits operating at different voltage levels, specialized voltage interface circuits are required. Level converters impose additional power consumption and propagation delay Overhead in a multi- system. High-speed and low power voltage interfacing is critical for effective power reduction with minimum effect on speed in a multi-VDD IC[3].

Several factors such as the path propagation delay statistics, the power and delay overhead of the level converters, and the availability and efficiency of the different power supplies determine the choice of the supply voltages in a multi-VDD system [5]. The number and the voltages of the multiple power supplies therefore vary with the type of the IC and the target set of applications. In this paper, a wide range of supply voltages are considered in order to address the speed, power, and area tradeoffs in the design of voltage level conversion circuits [10].

The level converters inertly on some form of feedback circuitry for controlling the operation of the pull-up network transistors in order to avoid static dc current within the level converter . These circuits, however, suffer from significant amount of short-circuit current and degraded speed characteristics due to the typically slow response of the feedback circuitry. Furthermore, to achieve functionality with a very low voltage transmitter, transistor resizing (significant increase in the device widths) is required in these feedback-based level converters, thereby further increasing the power consumption and the propagation delay [7].

In this paper, two new level converters based on a multi-V_{TH} threshold voltage CMOS technology are presented. Unlike the conventional level conversion techniques based on feedback, the proposed level converters eliminate the static dc current using multi- devices. The new level converters are compared with level converters in, for different supply voltages.

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The effectiveness of the proposed circuits for reducing power consumption is evaluated at scaled supply voltages down to the sub threshold regime.

The paper is organized as follows. The operation of the level converters is described in Section II. The power consumption characteristics and propagation delay of the level converters are presented in Section III. Simulation results carried out in section IV. Finally, some conclusions are provided in Section V.

II. LEVEL CONVERTERS

In this section various level conversion techniques are described. The issues related to the standard feedback-based level converters are discussed in Section II-A. Two new level converters based on a multi-V_{TH} CMOS technology are presented in Section II-B.

A. Feedback-Based Level Converters

The conventional feedback-based level converters are discussed in this section. When a low swing signal directly drives a gate that is connected to a higher supply voltage, the pull-up network of the receiver cannot be fully turned off. A receiver driven by a low voltage swing signal therefore produces static dc current. In order to suppress this dc current, specialized voltage interface circuits are employed between a low voltage driver and a full voltage swing receiver [2]. In the standard feedback-based voltage interface circuits, the pull-up network transistors are not directly driven by the low voltage swing signal provided by the driver. The operation of the pull-up network transistors is controlled by an internal feedback mechanism [4].

Isolated from the low voltage swing input signal, thereby avoiding the formation of static dc current paths within the Circuit. These traditional level converters, however, suffer from high short-circuit power and long propagation delay due to the typically slow response of the internal feedback circuitry that controls the operation of the pull-up transistors. Furthermore, the pull-down network transistors in these circuits are driven by low voltage swing signals unlike the pull-up network transistors that receive higher gate overdrive voltages from the full-voltage swing feedback paths. Particularly, at very low input voltages, the widths of the transistors that are directly driven by the low-swing signals need to be significantly increased in order to Balance the strength of the pull-up and the pull-down networks. This causes further degradation in the speed and the power efficiency of the conventional level converters when utilized with very low input voltages [3].

The standard feedback-based level converter (LC1) is shown in Fig. 1.M1 and M2 experience a low gate overdrive voltage (V_{DDL} -V_{TH}) during the operation of the circuit.M1 and M2 need to be sized larger to produce more current as compared toM3 and M4 , respectively, for functionality[2]. The circuit operates as follows. When the input is at 0 V M2 is turned off. Node1 is charged to V_{DDL}. M2 is turned on. Node3 is discharged to 0 V turning M4 On. Node2 is charged to V_{DDH} turning M3 off. The output is pulled down to 0 V. When the input transitions to V_{DDL}, M2is turned on. Node1 is discharged, turning M1 off. Node2 is discharged, turning M3 on. Node3 is charged up to V_{DDH} turning M4 off. The output transitions to V_{DDH}. A feedback loop, isolated from the input, controls the operation of M3 and M4 during both transitions of the output.

Due to the transitory contention between the pull-up and the pull-down networks and the large size of the NMOS transistors (M1 and M2), however, LC1 consumes significant short-circuit to maintain functionality with and dynamic switching power.

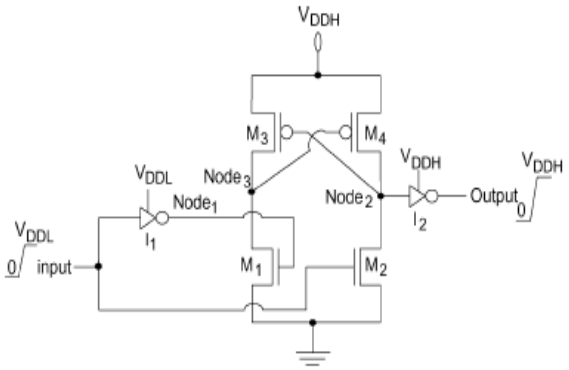

Fig.1. Standard level converter (LC1) presented in [2]. VDDL is the lower Supply voltage. VDDH is the higher supply voltages.

The lower values of V_{DDL}, the sizes of M1 and M2 need to be further increased in order compensate for the gate overdrive degradation. The load seen by the previous stage (driver circuit) is therefore increased, thereby further degrading the speed and increasing the power consumption. Tapered buffers are required to drive M1 and M2 at very low voltages. These tapered buffers further increase the power consumption of LC1.

Another level converter (LC2) is presented in for enhanced speed as compared to LC1. LC2 is shown in Fig. 2.M6 maintains the voltage of Node3 between V_{DDL} and V_{DDL} + V_{THN} in order to enhance the current produced by M1. The capacitor (C= 8 Ff) stabilizes the voltage of Node3 against the noise induced by the nearby switching events. The circuit operates as follows. When the input is at 0 V, Node1 is discharged through M1.M3 is turned on.M2 is turned off. Node2 is charged to V_{DDH}, turning M4 off. The output is discharged to 0 V. When the input transitions to V_{DDL}, M2 is turned on. Node1 is initially charged to a voltage between V_{DDL}-V_{THN} and V_{DDL} through M1.M3 is not completely cutoff (weakly active).M2 is sized to be stronger than M3 for the circuit to function properly [4]. Node is discharged, turning M4 on.Node1 is charged all the way up to V_{DDH}, thereby eventually turning M3 off. The output transition to V_{DDH}.

When the input switches from 0 V to V_{DDL} there is a direct current path from V_{DDH} to G_{ND} through the M2 – M3 path. This direct current path exists until Node1 is charged to V_{DDH} through M4 and M5. Similarly, when the input switches from V_{DDL} to 0 V, there is a direct current path from V_{DDL} to G_{ND} through the M5–M4 –M1 path. This direct current path exists until Node2 is pulled up to V_{DDH} and M4 is turned off. LC2 therefore consumes significant short-circuit power, similar to LC1, during both low-to-high and high-to-low transitions of the output. Furthermore, when V_{DDL} is reduced, a significant increase in the size of M2 is required for maintaining functionality.

The load seen by the driver circuit therefore increases at Lower V_{DDL}. Tapered buffers are required for driving LC2 at very low voltages. These tapered input drivers further increase the power consumption of LC2.

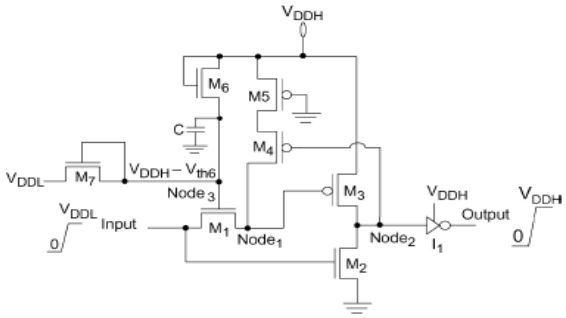

Fig. 2. Level converter (LC2) presented in [4].

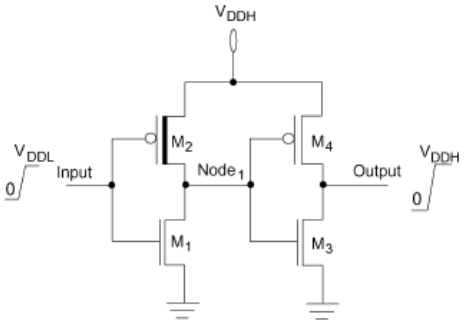

Fig. 3. First proposed level converter (PC1). Thick line in the channel area indicates a high-V_{TH} device.

B. Multi- Level Converters

Two new multi - V_{TH} level converters are described in this section. Unlike the previously published level converters that rely on feedback, the proposed level converters employ a multi-V_{TH} CMOS technology in order to eliminate the static dc current. The high threshold voltage pull-up network transistors in the new level converters are directly driven by the low-swing signals without producing a static dc current problem. The first proposed level converter (PC1) is shown in Fig.3 PC1 is composed of two cascaded inverters with dual -V_{TH} transistors. The threshold voltage of M2(Vth-M2)is more negative (higher V_{TH}) for avoiding static dc current in the first inverter when the input is at V_{DDL} .V_{th}-M2 is required to be higher than V_{DDH}-V_{DDL} for eliminating the static dc current. PC1 operates as follows. When the input is at 0 V, M2 is turned on. M1 is cutoff.Node1 is pulled up to V_{DDH}. The output is discharged to 0 V. When the input transitions to V_{DDL}, M1 is turned on. M2 is turned off since VGS, M2>V_{TH}, M2 .Node1 is discharged to 0 V. The output is charged to VDDH [11].

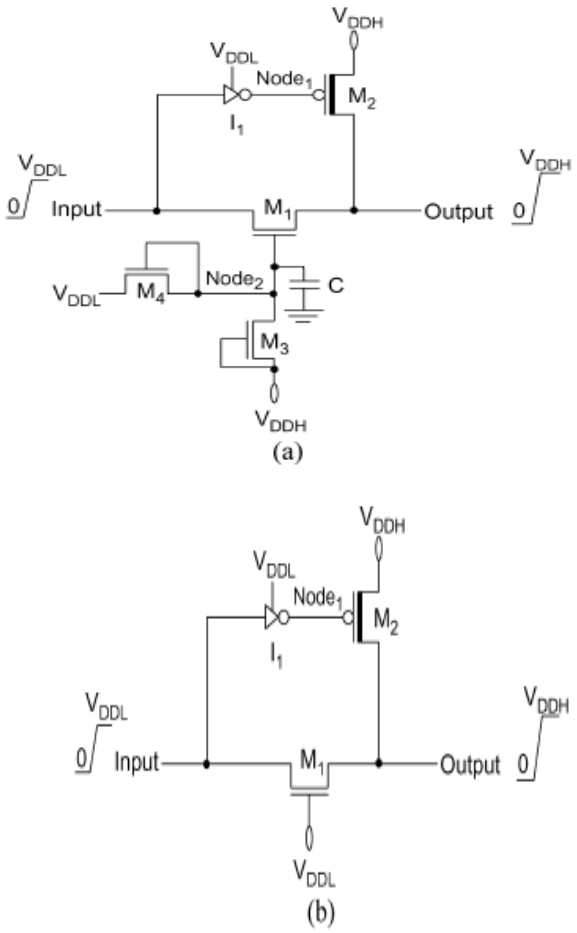

Fig. 4.Second proposed level converter (PC2). Thick line in the channel area indicates a high-V_{TH} device. (a) Circuit configuration for V_{DDL} and V_{DDH} that satisfy both (1) and (3). (b) Circuit configuration for the supply voltages that do not satisfy either (1) or (3).

PC1 has fewer transistors as compared LC1 and LC2. Furthermore, the elimination of the slow feedback circuitry reduces the short-circuit power of PC1 as compared to LC1 and LC2. For the lower values of V_{DDL}, the threshold voltage of M2 needs to be more negative (higher-V_{TH}) in order to suppress the static dc current. Provided that a multi-

V_{TH} CMOS technology is available, no increase in the size of M1 is required for achieving functionality at lower input voltages with the proposed circuit (unlike LC1 and LC2). Therefore, particularly for the very low values of V_{DDL}, PC1 consumes lower power, occupies significantly smaller area, and imposes a much smaller load capacitance on the input driver as compared to LC1 and LC2. The circuit configurations of the second proposed level Converter

(PC2) for operation at different supply voltages are shown in Fig. 4. |Vth-M2| is required to be higher than V_{DDH}-V_{DDL} for eliminating the static dc current when the Input is low (Node1 is at V_{DDL}). M1 needs to be cutoff after a "1" is successfully propagated to the output (the input is at

V_{DDL} and the output is at V_{DDH}) in order to avoid the formation of a static dc current path between V_{DDH} and V_{DDL} through M1.The peripheral circuitry composed of M3, M4 , and C, shown in Fig. 4(a).

PC2 operates as follows. When the input is at 0 V, Node1 is pulled high to V_{DDL} turning off M2 (note that M2-V_{th} has a high- V_{TH}). The output node is discharged to 0 V through the M1 pass transistor .When the input transitions to V_{DDL} , the output node is initially charged to V_{DDH}-Vthn-M1-Vthn-M3 and V_{DDL}-Vthn-M1 through M1 with the circuit configurations shown in Fig. 4(a) and (b), respectively. M2 is turned on after the high-to-low propagation delay of the inverter (I1). The output is pulled high all the way up to V_{DDH} through M2[9]. M1 is turned off isolating the two power supplies. Both M1 and M2 assist the output low-to-high transition, thereby eliminating the contention current and enhancing the low-to-high propagation speed. The small transistor count and the elimination of the feedback reduce the power consumption of the proposed level converter as compared to LC1 and LC2. Furthermore, the speed of PC2 is enhanced due to the shorter input-to-output signal propagation path (composed of only one pass transistor) and the elimination of the contention current during the output low-to-high transition [6].

III. SPEED & POWER CONSUMPTION CHARACTERSTICS

In this section, the two new level converters are compared to level converters in [7], for average power consumption and propagation delay.

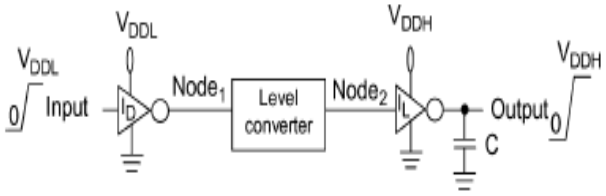

Fig. 5. Simulation setup for characterizing the level converters. Power is measured for the entire test circuit including the driver and the load inverters.

The proposed level converters and level converters are placed in the level converter in the figure 5. The average power and propagation delay for each and every level converter are calculated. The simulations are carried out for the following values of V_{DDL}: 0.5, 1, and 1.2 V. The standard Nominal-V_{TH} supply voltage (V_{DDH}) is 1.8 V in this 0.18-µm CMOS technology. The design and optimization are carried out using HSPICE built in optimizer in a 0.18-µm TSMC CMOS technology. The average power and propagation delay of the proposed level converters are compared with the level converters in [7]. By varying the input supply voltage V_{DDL} and constant output voltage V_{DDH} proposed circuit offers significant power aging and enhanced speed. The readings are tabulated in the table I.

TABLE I Average Power Consumption And Propagation Delay Of The Level Converters

V_{DDL}	V_{DDH}	NAME OF THE LEVEL CONVERTERS	OPTIMUM POWER DESIGN P in (µW)	OPTIMUM DELAY DESIGN D in (PS)
.5v	1.8v	LC1	9.133	4529
		LC2	0.300	3413
		PC1	0.308	1030
		PC2	0.308	1720
		LC1	7.97	257
1v	1.8v	LC2	6.23	197
		PC1	2.15	165
		PC2	1.72	153
1.2v	1.8v	LC1	5.97	203
		LC2	5.82	176
		PC1	2.11	137
		PC2	1.67	103

The higher threshold voltage for transistor M2 in proposed circuits is given in such a way that threshold voltage of M2 is more negative and it should be higher than the difference in value of V_{DDH}-V_{DDL} (higher V_{th}) for avoiding static dc current in the first inverter when the input is at V_{DDL}.

TABLE II OPTIMUM THRESHOLD VOLTAGES WITH THE PROPOSED LEVEL CONVERTERS

V_{DDL}	V_{DDH}	NAME OF THE CIRCUIT	NAME OF THE TRANSISTOR(M 2)
.5V	1.8V	PC1	-1.50
		PC2	-1.44
1V	1.8V	PC1	-1.
		PC2	-0.96
1.2V	1.8V	PC1	-0.84
		PC2	-0.82

IV. SIMULATION RESULTS

In this section a common waveform and peak power characteristics of the level converter has given. The input V_{DDL} is 0.5V, 1V and 1. 2V. the output V_{DDH} is 1.8v.the V_{DDH} is standard nominal supply voltage in a 0.18µm TSMC CMOS technology. The proposed level converters peak power characteristics are compared with the level converters in [8]. The figure 9,10,11,12 shows that the proposed level converters offers the significant power saving of 70% and gives the high peak power characteristics compare to of other level converters in [7].

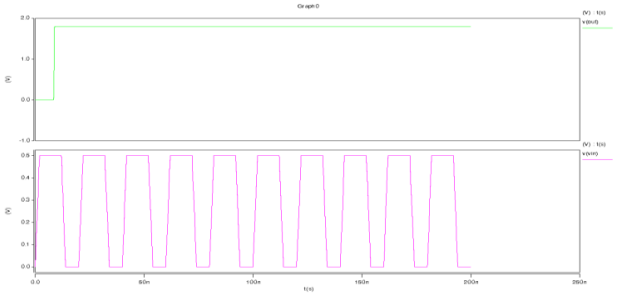

Fig.6 Power dissipation at V_{DDL}=0.5V and V_{DDH}=1.8V

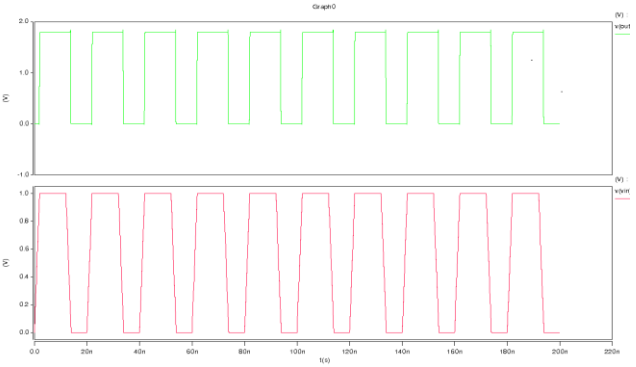

Fig.7 power dissipation at V_{DDL}=1v and V_{DDH}=1.8v

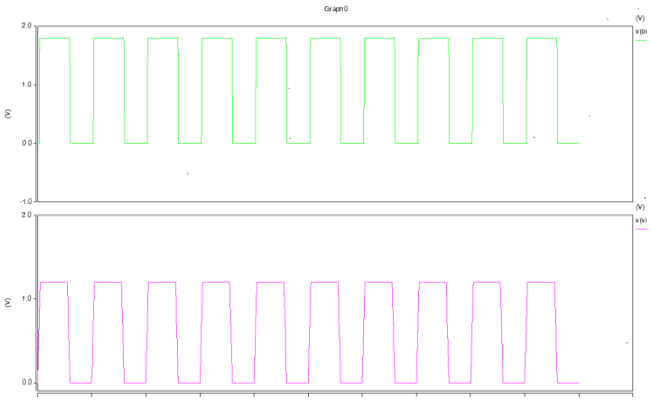

Fig.8 power dissipation at V_{DDL}=1.2v and V_{DDH}=1.8v

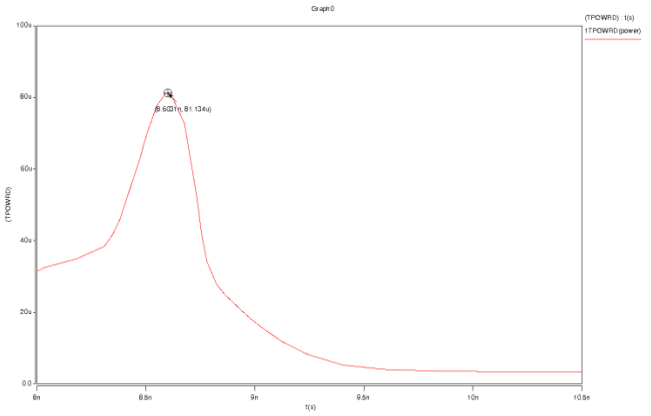

Fig.9 peak power for Level Converter LC1

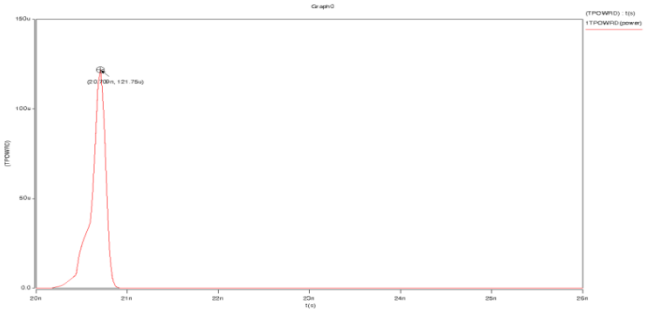

Fig.10 peak power for Level Converter LC2

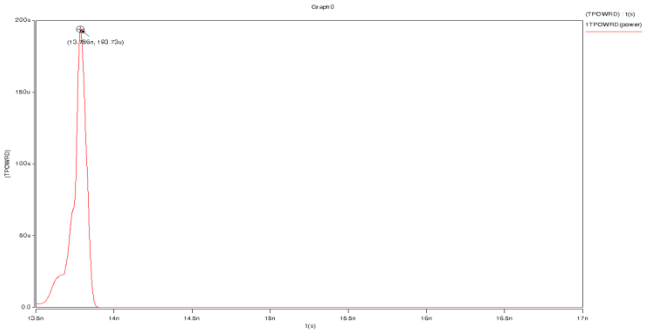

Fig.11 peak power for Level Converter PC1

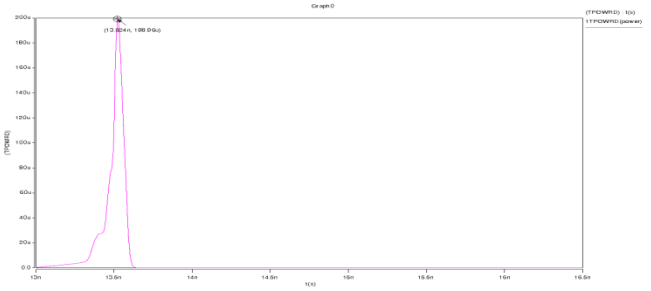

Fig.12 Peak power for Level Converter PC2

V. CONCLUSION

Two new level converters based on a multi-V_{TH} CMOS technology are proposed. Unlike the standard level converters based on feedback, the new circuits employ multi-V_{TH} transistors in order to suppress the dc current paths in CMOS gates driven by low-swing input signals. The proposed level converters are compared with the previously published circuits for different values of the lower supply voltages in a multi-V_{DD} system. When the circuits are individually optimized for minimum power consumption in a 0.18- m TSMC CMOS technology, the proposed level converter offers significant power saves and enhance speed compare to the level converters in.

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Dr.S.Manikandan. .E.,M.Tech(Hons).,Ph.D(U.K).,Ph.D(India).,MPSLV., is a personality with versatile skills both in the field of academic and administration. He has more than twelve years teaching experience excluding five years in the field of research. He is also an academician with foreign exposure. He has taught in European university of LEFKE, Cyprus. He has published more than twenty research articles in various reputed journals. He is also a reviewer and has received the articles in more than seveninternationaljournals. He has guided twelve PG students (both M.E & M.Tech) in their research pursuit. Apart from all these things he is an expert in the field of interactive teaching and aims at promoting quality education in an interactive way in contradiction with the traditional 'One man show' in the class rooms. At present, he is a research supervisor for doctoral scholars, besides continuing his service both in the field of academic and administration.