A Survey of Logic Based Distributed Routing for On-Chip Interconnection Networks

Naveen Choudhary, Chand Mal Samota

Abstract—The availability of increased number of resources on a single silicon chip is enforcing the designers to come up with mechanisms for efficient and effective management of these resources on a chip. Moreover defective components, chip virtualization and power-aware techniques may lead to irregular on chip interconnection topology making efficient routing a non trivial challenge. Nearly, all routing algorithms and topologies support switches that make use of routing tables for efficient routing. However memories do not scale well in terms of area and power consumption for the routing tables, thus not practical for scalable on chip networks.

Logic based distributed routing (LBDR) is recently proposed as an alternative solution to the table based distributed routing which can drastically reduce the memory requirement even while being as efficient as table based distributed routing. LBDR is a simple methodology of routing that enables the removal of the routing tables at every switch and uses only a small set of bits per switch to enable efficient routing. This paper surveys different variations of efficient Logic-based distributed routing (LBDR) proposed in the NoC research literature for regular and irregular on chip interconnection topologies.

Index Terms— Networks-on-chip, Routing, LBDR, LBDRe, uLBDR, Fault-tolerance.

I. INTRODUCTION

The packing density in deep sub-micron technology doubles every 18 months as per Moore's Law, leading to increased research interests in the domain of network-on-chip (NoC) interconnection paradigm that provides suitability, flexibility and scalability in designing efficient SoCs. A paradigm shift from single core architectures to multi core architecture has been introduced in industries for designing high performance systems. According to the International Technology Roadmap for Semiconductors (ITRS) [1], before the end of this decade we will be entering the era of a billion transistors on a single chip. This gives a clear indication that in the near future we probably have devices ranging from mere mobile phones to adaptable mobile-devices with complex functions. As the number of on-chip transistors increases significantly and so does the complexity of integration.

With the increasing number of on-chip cores, certain challenges also arise and these issues must be catered well to maintain the performance and functionality of a the system. Several challenges such as effective chip utilization, voltage/frequency islands and manufacturing defects, efficient power saving techniques have been recognized by the researchers. Due to the presence of manufacturing defects, certain links or node become disable and a regular topology becomes an irregular one

Routing of communicating packets can be implemented in different ways in Network on Chip (NoCs). Different types of routing methodologies such as source and distributed routing are available for regular and irregular NoC topologies. Some instances of NoC routing algorithms can be enumerated as dimension order routing (DOR) for regular topologies and segment based routing(SR), up*/down* routing for irregular topologies. These routing schemes have some pros and cons. DOR results in reduced latency, power and area requirements but as the integration complexity grows it introduces a number of communication reliability issues. Segment based routing methodology offers flexibility [9]. Different segmentation processes and routing restriction policies result in fast-computation of many deadlock free algorithms. [4] proposed an organized segmentation process that achieves reliable performance with low variability for all topologies under uniform traffic conditions. Up*/Down* routing scheme is used in irregular topologies to provide a deadlock-free path but it may route packets over non-minimal paths [5].

Distributed Table based routing schemes have also been proposed to deal with irregular topologies and can be used in application-specific systems which facilitates the use of any topology with any routing algorithm. It also serves the purpose of fault-tolerance in routing. However, it does not scale well with area which is a important design constrain.

To provide better support for routing in both regular and irregular topologies without the need of routing tables, a Logic based distributed routing (LBDR) has been proposed [2] This routing scheme is based on the computation of three bits per output port (2 bits for routing restriction and 1 bit for connectivity) at every switch and a small logic block containing several gates. This is an efficient algorithm requiring minimum logic and is table-less requiring minimized area overheads.
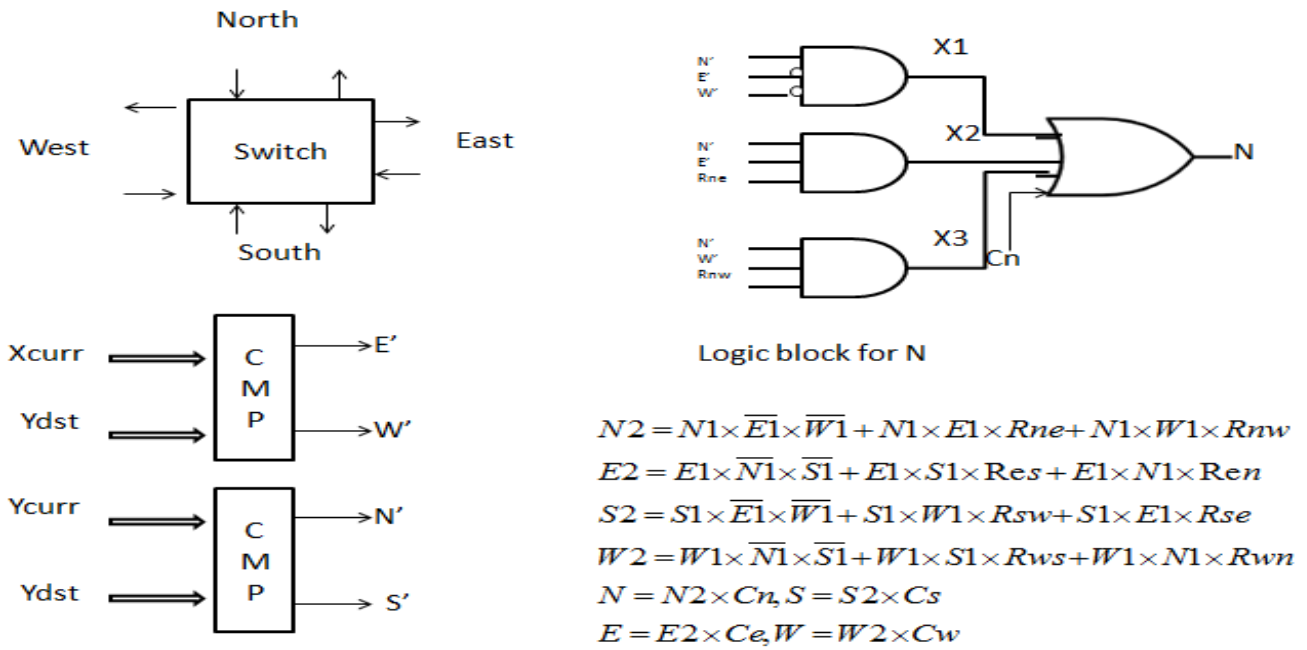
Fig. 1 Logic calculation for LBDR method

In this paper, we have surveyed LBDR and its various variations proposed in the research literature of NOC domain. The rest of paper is organized as follows: section II discusses the challenges encountered in existing routing techniques and also presents the motivation behind the LBDR. Section III briefly presents the principle and technique for implementation of LBDR. Next the paper discusses the various variations of LBDR in subsequent sections (IV-VII). Lastly, in section VIII we conclude.

II. ON-CHIP NETWORK ROUTING CHALLENGES

Reduction in memory requirement: The main drawback of table based routing techniques is that memories do not scale in terms of power, latency and area and this becomes a bottleneck as number of on-chip cores grow. Routing tables are expensive in terms of access time and resources, and feature poor scalability properties. Several solutions have been suggested for memory requirement reduction such as Interval Routing [6], The FIR method [7], *street-sign routing* [8] for regular topologies and Region based routing [14], [15] for irregular topologies. However none of these routing schemes allows implementing the distributed routing in irregular topologies with minimum logic and no routing tables.

LBDR has come up as a promising solution to mitigate the above mentioned issues. It minimizes logic and the memory requirement by adopting table-less routing scheme which is also deadlock free.

III. LOGIC-BASED DISTRIBUTED ROUTING

Logic-Based Distributed Routing (LBDR) [2] gives a new perspective of scalable and efficient routing implementation for regular and irregular topologies. It allows the use of any distributed routing algorithm without maintaining the routing tables.

In this routing scheme, each router has to keep knowledge of its position in the architecture and should be able to determine what direction it is from the destination. This information saves the storage requirement over table or buffer. The information is used to route the packet based on a small number of bits and requires only a few logic gates per router. [2] presents an efficient and scalable LBDR implementation, but its scope is limited to some specific sub-topologies created due to specific set of faults in 2D Mesh such as 'p', 'q', 'd', 'b' and '+' because in these topologies, the end nodes can communicate with each other through a minimal path defined in original 2D mesh topology. This LBDR implementation (Fig. 1) is based on twelve bits. There are four output ports at each switch. Each output port requires three bits. Among these three bits, one bit is used as connection bit (C_x) and remaining two bits are used as routing restriction bits (R_{xy}). Values of these bits are computed offline.

R_{xy} ((x, y) $\in$ {E, S, W, N} and (x, y) are in different directions), indicates whether packets routed through some ports can make a turn at next hop. Connection bit is denoted by C_x (one of C_n, C_e, C_s, and C_w), and indicates whether a connection to the neighboring node is available through this port. e.g. the restriction bits at S output port is denoted as R_{se} and R_{sw}. These bits indicate whether packets routed through S port can take E or W as the output port at next switch and a connection bit corresponding to south port i.e. C_s is used. Routing logic of LBDR alternates in three steps as given below:

1. The relative position of destination node is computed using two comparators and coordinates of the current switch and destination switch located in the message header. *Direction signals* are also computed.
2. Based on both the output of first step and the routing restrictions, output ports are calculated as shown in Figure 1.

3. Next, the Connectivity bit corresponding to each output port (from step 2) is checked to determine whether a connection to the neighboring node is available through this port.

While the potential advantages of LBDR are certainly compelling, the following limitations have curtailed its adoption as a mainstream technology:

1. LBDR can operate in presence of faulty nodes if such nodes can only be located at four corners of the mesh topology.
2. LBDR's visibility is limited to single hop only.

IV. EXTENDED LBDR

In [3] a variation of LBDR i.e. LBDRe, is proposed which overcomes one of the limitation of LBDR by extending the visibility to two hops. The LBDRe implementation is based on twenty four bits. There are four output ports at each switch. Each output port requires six bits.

Restriction bit is denoted by R_{2xy} which indicates that whether the y direction can be taken two hops away from the current switch through the x direction. All the restrictions followed by LBDR are also followed by LBDRe.

LBDRe extends the functionality of LBDR by computing four extra signals to gain two hop visibilities. This routing scheme can be used with SR_h (segment based) routing [3] without loss of performance.

V. BROADCAST LBDR

bLBDR [13] fulfills all the practical requirements. It is efficient in terms of latency, power and area. It provides support for virtualization, partitionability, fault-tolerance, traffic isolation and broadcast across the entire network as well as constrained to coherency domains or regions. All this is achieved by a small and power efficient routing logic.

In this approach Virtual cut-through (VCT) switching is adopted to avoid tree-based deadlock issues and if virtual channels are drawn in to avoid deadlocks, wormhole switching can also be used.

S. Rodrigo et al. has presented the bLBDR mechanism in [13]. bLBDR extends LBDR functionality in two directions. First by providing broadcast and multicast support within the NoC and secondly by defining regions and isolating the traffic within a given region. The broadcast/multicast mechanism does not require any new information at switches and end-nodes. Only a small logic is required to create the broadcast tree at each switch. This mechanism operates by broadcasting packets at the region level. Any of the nodes contained within a region defined by the connectivity C_x bits can initiate the broadcast operation. The packet which is being broadcasted can be received at the nodes contained within a region only. For avoiding duplicity, every destination node can receive only one packet. The bLBDR can be applied to any routing/topology combination where LBDR is used. Also, any region pattern compatible with LBDR can be used. However bLBDR doesn't work well in networks where destinations are spread out far and wide.

VI. UNIVERSAL LBDR

uLBDR [10] implements routing for any 2-D mesh topology. It does not require any routing table. For facilitating routing around faulty links, it adds logic to each input port.

This approach requires virtual cut-through switching where entire packet is buffered at each router. Other solutions handle permanent faults by flooding the network to overcome lost network connections, which results in a high performance overhead [16] [17]. Stochastic approaches [18], [19] provide fault tolerance by means of a probabilistic broadcast mechanism. Immunet [20] routes packets adaptively toward their destinations, based on buffer availability. Reserved, escape and virtual channels are used to guarantee that packets will reach their destination and avoid faulty links.

As highlighted in [12], LBDRdr extends greatly the coverage. However, there are subtle cases that are still not covered by LBDRdr.
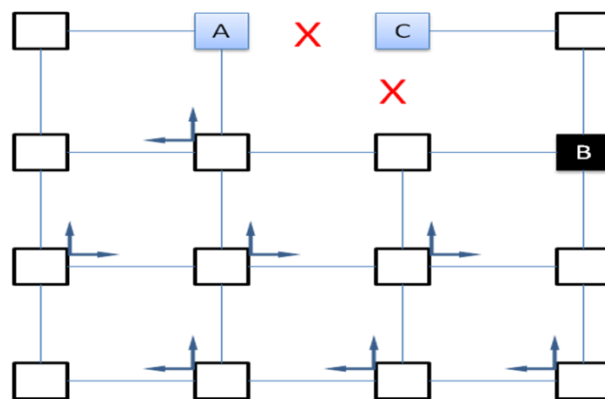

Fig. 2 Faults in 2D mesh in SR_h routing

Fig. 2 shows an example of the problem which comes by the fact that for some destinations located at the same quadrant, at router B the routing engine should provide one port (*N*) for some destinations (router *C*) and another port (*W*) for other destinations (router *A*). As LBDR (or *LBDRdr*) works in quadrants, there is no way to indicate the router regarding which option should be given to the message.

To solve this problem, [12] introduce the FORKS module. The FORK [12] extension along with DEROUTES extension and the LBDR module results into the formation of the uLBDR mechanism. The objective is to replicate the message through two output ports. It depends on four additional configuration bits (fork bits): *Fn*, *Fe*, *Fw*, and *Fs*. The output ports that must be used to fork a packet is reflected by the bit configuration set on these bits. Whenever a packet arrives and its destination is checked. If destination is in the same quadrant defined by the fork bits, then the packet needs to be forked.

The *FORK* signal is set and forwarded to the arbiter to distinguish between two possible valid routing options. *Fn*, *Fe*, *Fw*, and *Fs* bits are set appropriately. In case of irregularity in the network topology where at least one pair of end nodes could not communicate through one path, the bit computation algorithm tests any possible fork operation at routers where no deroute succeeded, again discarding any possible choice that leads to cross a routing restriction. Fork options are computed offline.

When two fork messages compete for the same set of resources, Deadlock may occur in wormhole switching

The solution of this problem is to use virtual cut-through (VCT) Switching since the buffer requirements in a VCT switch do not depend on the implementation of FORK operations. Note also the buffer

VII. LBDR EXTENSION

LBDRx [11] proposes a mechanism which is extension of the basic LBDR. LBDRx facilitates full coverage to all the complex irregular and application specific networks. LBDRx mechanism enhances the connectivity of switches from four switches port connected to one switch to 20 ports for connecting to other switches. It extends the visibility of hops to three so that any of these ports can be configured as a 1-hop port, a 2-hop port, or a 3-hop port. According to hop visibility 20 different directions are supported for the ports and each port can be configured to any of 20 directions. All possible directions are: Four directions for 1-hop (N, E, W, S), eight directions for 2-hop (four diagonals and four straight directions) and eight directions for 3-hop(NNW,NNE, WWN,WWS,SSW,SSE,EES,EEN). Fig. 3. shows all the 20 possible directions supported by LBDRx.
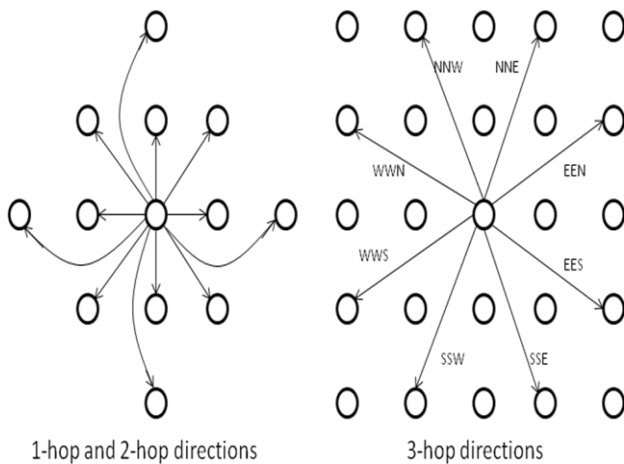

Fig. 3 Possible directions for LBDRx

Routing logic of LBDRx is alienated into two parts: (1) the relative positions of destination node is computed using two comparators and coordinates of the current switch and destination switch located in the message header. Direction signal are also computed simultaneously. (2) In the second part, the logic is divided in three parts in order to address the logic for the different type of output ports (1-hop, 2-hop, and 3-hop ports). The 3-hop ports have the highest priority followed by 2-hop ports. To implement this priority scheme, two control signals ($2hop$ and $3hop$ signals) are used.

LBDR approach is extended to LBDRx to cover complex topologies derived from SoC designs, thus enabling the use of the LBDRx approach in application-specific SoC systems. J.Cano et al. in [11], [21] has also proposed a tool to map the initial irregular topology into a logical regular structure where the LBDRx approach can be used.

VIII. CONCLUSION

In this paper a survey of Logic Based Distributed Routing (LBDR) methodologies and its variations such as LBDRe, uLBDR, bLBDR, LBDRx proposed in the research literature of NoC domain is presented. Logic Based Distributed Routing is able to cater the needs of regular as well as irregular NoC topologies. LBDR efficiently minimizes logic and the memory requirement by adopting table-less routing functionality leading to reduced area overheads. Moreover LBDR routing is scalable and deadlock free which is a necessary requirement for future NoCs.

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