Low Voltage, High Bandwidth & Input Impedance CMOS Differential Amplifier at NANO Scale

Adil Zaidi, Divakar Veer Vikram Singh, Firoz, Dileep Kumar, Veerandra Pratap

Abstract*— Since analog circuits have proved primarily essential in many of today's high complex performance systems. This paper demonstrate designing and simulation of low power CMOS technology based differential amplifier at nano scale of different channel length(45nm,32nm,22nm) via applying various supply voltages i.e. 1.1V, 0.95V , 0.9V respectively. Here the high input impedance, low power dissipation circuit is mainly characterized in terms of common mode rejection ratio (CMRR), voltage gain and gain band width product .The input impedance calculated are in the range of 190 GΩ (giga ohm), cut off frequency (-3db) approximately greater than 50 MHz (mega hertz) and average power dissipation in the order of less than 130 µw (micro watt). The simulation result shows that all transistors are operated in saturation region, with this unique behavior of MOSFET transistor operating in this region not only allows a designer to work at a low voltage but also at a high frequency. Finally, the analog design consists of low operating voltages via very deep sub micron (nano scale) technology.. The simulation is carried out using PTM Low Power 45nm, 32nm, & 22nm Metal Gate / High-K / Strained-Si technology with H-spice. A Matlab tool is also used to plot the graph of various parameters at different channel length in two dimensions (2-D).

***IndexTerms*—Very deep sub-micron (VDSM), Nanoelectronics, Scaling.**

I. INTRODUCTION

The great progress toward building electronic circuits integrated on the nanometer scale has opened the possibility for shrinking drastically the size and power consumption of large-scale, general-purpose electronic memories and processors. These recent advances in nano fabrication and nano electronics could have conspicuous, pervasive impacts for general purpose computing in several years time. However, these advances also make it possible to shrink the form factor and power requirements for a wide class of much simpler circuits.

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Adil Zaidi Assistant Professor in the Department of Electronics and communication Engineering, CET-IILM-AHL, GreaterNoida Uttar Pradesh, India.

Divakar veer Vikram singh is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had done his summer training from B.H.E.L IP Jagdishpur, Sultanpur U.P. India.

Firoz is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had done his summer training from B.H.E.L IP Jagdishpur, Sultanpur U.P.India.

Dileep Kumar is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had done his summer training from B.H.E.L IP Jagdishpur, Sultanpur U.P. India.

Veerandra pratap is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had done his summer training from CETPA Noida U.P. India.

Such circuits often are dedicated to specialized applications in the control and monitoring of other systems [1]. CMOS technology has been widely used for various RF applications, such as cellular phone, WLAN, and Bluetooth, due to its super integration scale and powerful on-chip digital signal processing capability [2].The demand of low voltage, low power and high performance are great challenges for the engineering of sub 50nm gate length. CMOS device of the increasing interest and necessities of nomadic electronic systems [3].

Designing high performance analog integrated circuits is becoming increasingly exigent with the relentless trend toward reduced supply voltages and transistor channel length. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. The feature size of individual transistor is shrinking from deep sum-micrometer (DSM) to even nanometer region. As the scale of integration improves, more transistors, faster and smaller than their predecessors, are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip [4,5,6,7]. Impact of scaling is characterized in terms of several indicators:

- Minimum feature size
- Number of gates on one chip
- Power dissipation
- Maximum operational frequency
- Production cost

The differential amplifier is one of the most versatile circuits used in analog circuit design. These are widely used in the electronics industry and are generally preferred over their single-ended counterparts because of their better common-mode noise rejection, reduced harmonic distortion, and increased output voltage swing. Differential amplifiers are used to amplify analog as well as digital signals, and can be used in various implementations to provide an output from the amplifier in response to differential inputs [2]. Current mirrors are used extensively in CMOS analog circuits both as biasing elements (NMOS) and as active loads(PMOS) to obtain high AC voltage gain enhancement mode transistors remain in saturation when the gate is tied to the drain($V_{D=}V_G$) [4,9,10].

$$V_{DS} > V_{GS} - V_{th} \qquad (1)$$

Based on Eq.1 constant current sources are obtained through current mirrors designed by passing a reference current through a diode-connected (gate tied to drain) transistor.

Figures 1.1 and 1.2 show the p-MOS and n-MOS current mirrors design. A p-MOS mirror serves as a current source while the n-MOS acts as a current sink.[8,11] The voltage developed across the diode-connected transistor is applied to the gate and source of the second transistor, which provides a constant output current. Since both the transistors have the same gate to source voltage, hence both transistors will be in the saturation region. The current ratio I_{OUT}/I_{REF} is determined by the aspect ratios of the transistors. For identical sized transistors, the ratio is unity, which means that the output current mirrors the input current. Because the physical channel length that is achieved can vary substantially due to process variations, the accurate ratios usually result when devices of the same channel length are used, and the ratio of currents is set by the channel width [11].

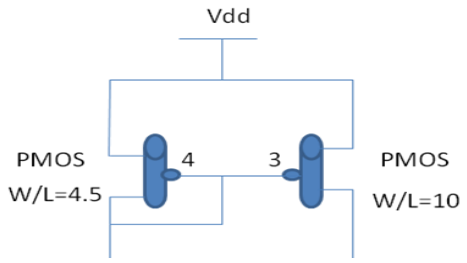

Fig.1.1 Active load (P-MOS current mirror)

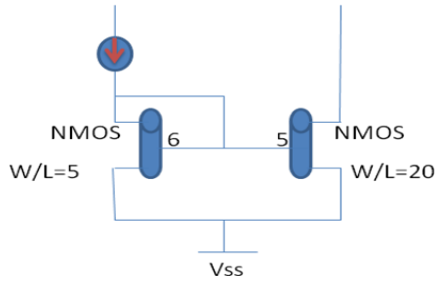

Fig.1.2 Bias element (N-MOS current mirror)

This manuscript investigates a high impedance, low power and high bandwidth differential amplifier dc, transient and ac analysis designed at 45nm, 32nm, 22nm respectively where DC analysis explain the transfer characteristics (output voltage versus input voltage), transient analysis describes time domain approach and AC analysis includes frequency domain study .

The paper is classified as follows: section II includes the modeling of differential amplifier at nano scale. Section III describes simulated characteristics i.e. DC, Transient & AC analysis curves at different channel length (45nm, 32nm, 22nm) in nanometer range correspondingly. Section IV includes results and discussion, section V contains acknowledgement followed by references in section VI.

II. MODELING & DESIGNING OF CMOS DIFFERENTIAL AMPLIFIER AT NANO SCALE

The objective of the differential amplifier is to amplify the difference between two different potentials regardless of common mode value. For ideal differential amplifier, the common mode gain is zero which makes the CMRR infinite. The input offset voltage is also zero for the ideal case. The active load differential amplifier has better performance only if all transistors are identical. The use of identical transistors leads to no mismatch, hence offset voltage becomes zero, but practically it is not possible .Practical differential amplifiers have non-zero common mode gain, therefore, the CMRR becomes finite and they have non-zero offset voltage. The circuit arrangement for CMOS differential amplifier with active load and single ended output is shown in Figure. 1. To achieve better performance in voltage gain, bandwidth and gain bandwidth product, all transistors should be in saturation region.[5,12,13].CMOS design is becoming increasingly blurred, especially with the challenges presented by very deep sub-micron (VDSM) fabrication technologies, very low operating voltages , and operating frequencies extending well into GHz range while analog figure of merit, such as transistor gain and output swing are degraded [5,6,12,14]

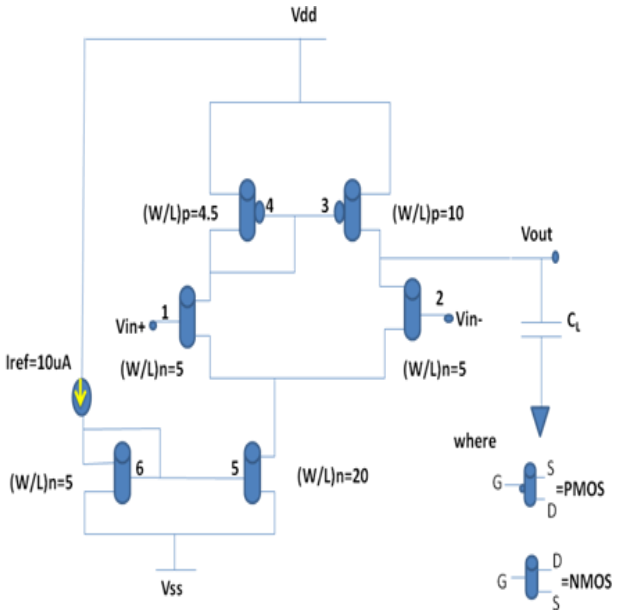

Fig2.1 CMOS DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

The differential amplifiers are used to amplify analog as well as digital signals, and can be used in various implementable applications so as to provide an output from the amplifier in desired response to the differential inputs. It is also very compatible with integrated circuit technology and serves as the input stage to most of operational amplifier. These circuits can be readily adapted to behave as an operational amplifier, a comparator, an instrumentation amplifier, etc. The differential amplifier is often a building block or sub-circuit used within high-quality integrated circuit amplifiers, linear and nonlinear signal processing circuits, and even certain logic gates and digital interfacing circuits in various VLSI applications.

Differential amplifier gain-

$$A_d = \frac{v_o}{v_{id}} = g_m(R_D // r_o)$$

Where:-

$A_{d=}$differential gain, $V_{o=}$ output voltage, $V_{id=}$ differential input, $g_{m=}$ transcondutance, $R_{D=}$ drain resistance, $r_{o\ =}$output resistance

Common mode gain:-

$$A_{cm1} = A_{cm2} = \frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = -\frac{R_D}{\frac{1}{g_m} + 2R_{ss}} \cong -\frac{R_D}{2R_{ss}}$$

Where:-

A_{cm1}=A_{cm2}=common mode gain

R_{ss}= *source resistance*

CMRR (Common mode rejection ratio):-

$$CMRR \equiv \left|\frac{A_{d1}}{A_{cm1}}\right| = \left|\frac{A_{d2}}{A_{cm2}}\right| = g_m R_{ss}$$

III. SIMULATION CHARACTERISTICS

H-spice tool is used for simulation of CMOS differential amplifier. Apart from this matlab tool is also used for plotting graph in ac analysis. Simulation section is divided into three parts: - DC, transient, and AC analysis at 45nm, 32nm, 22nm respectively.

1) DC ANALYSIS:-

1.1 Input parameters

Technology	At 45nm	At 32nm	At 22nm
V_{id}	0.1v	0.1v	0.1v
R_L	100K	100K	100K
C_L	100f	100f	100f
V_{dd}	1.1V	0.95V	0.9V
V_{ss}	-1.1V	-0.95 V	-0.9V
Iref	10u	10u	10u

1.2 DC transfer curves

The differential mode curve is linear for input voltage between -400mV and +400mV. So the present circuit is suitable for low voltage applications. Differential amplifier is in the balance condition that's why output of differential amplifier is zero for zero differential input shown in the figure 3.1, 3.2 and 3.3 at 45nm, 32nm and 22nm respectively.

Small signal transfer characteristic			
Technology	**At 45nm**	**At 32nm**	**At 22nm**
V(5)/Vid	4.08	2.79	1.74
Input Resistance	269.21G	195.41G	231.40G
Output Resistance	28.64K	30.65K	32.46K

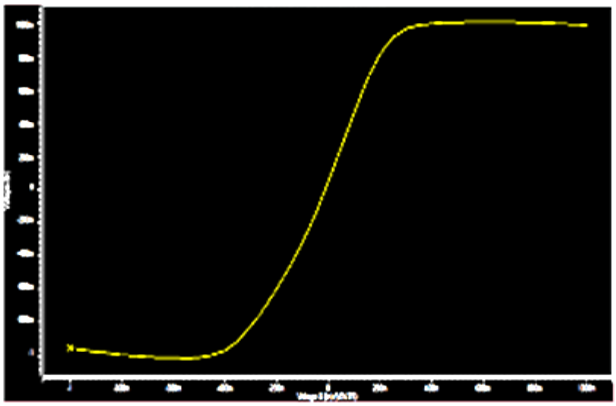

Fig.3.1 at 45nm

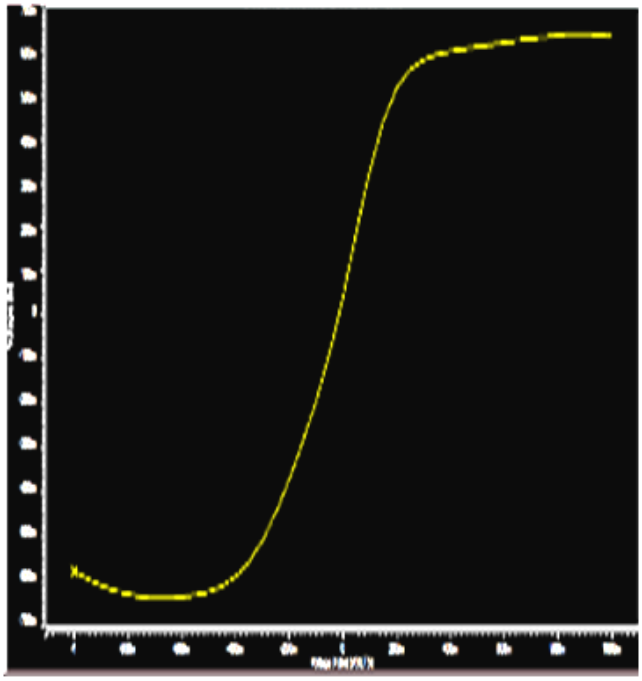

Fig.3.2 at 32mn

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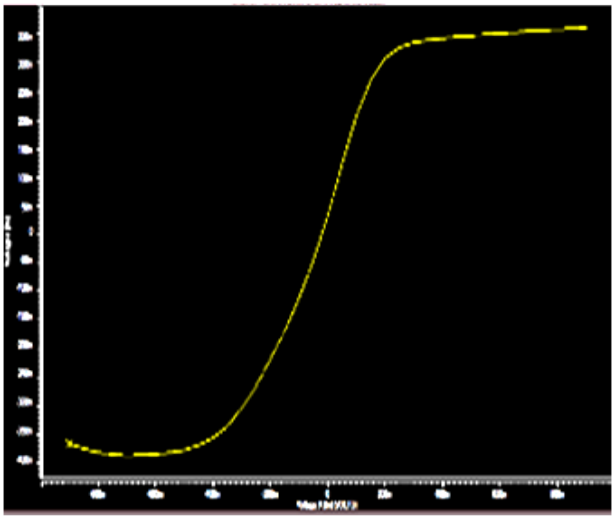

Fig.3.3 at 22nm

DC transfer characteristic

1.3 Output parameter

1.4. Internal parameters

The various internal parameters mentioned in TABLE 1.1 shows that with the decrease in channel length from 45nm to 22nm value of Vth, increase and the value of C_{gs} and C_{gd} decreased.

Currents: **Id**.
Voltages: **Vgs, Vds, Vth, Vdsat.**
Transconductance: **gm**.
Capacitances: **Cgd, Cgs,**
Current gain: Beta.
various subscripts indicates:
g for gate terminal
d for drain terminal
s for source terminal
th for threshold
sat for saturation

Technology	At 45nm	At 32nm	At 22nm
V_{in}	0.1v	0.1v	0.1v
R_L	100K	100K	100K
C_L	100f	100f	100f
V_{dd}	1.1V	0.95V	0.9V
V_{ss}	-1.1V	-0.95V	-0.9V
Iref	10u	10u	10u

TABLE 1.1

CMOS DIFFERENTIAL AMPLIFIER AT 45nm (DC analysis)						
MODEL	NMOS-1	NMOS-2	PMOS-3	PMOS-4	NMOS-5	NMOS-6
REGION	SAT	SAT	SAT	SAT	SAT	SAT
i_d	22.27u	17.74u	-22.28u	-18.24u	40.02u	10.00u
V_{gs}	682.26m	682.26m	-711.74m	-711.74m	703.38m	703.38m
V_{ds}	1.38	1.04	-711.74m	-1.04	106.38m	703.38m
V_{th}	537.72m	558.71m	-536.33m	-511.93m	616.87m	579.83m
V_{dsat}	135.22m	124.68m	-171.10m	-186.03m	106.98m	125.09m
beta	2.54m	2.50m	1.48m	970.06u	9.84m	1.42m
g_m	188.70u	168.69u	189.54u	137.16u	418.84u	95.78u
c_{gs}	250.98a	245.27a	499.28a	325.48a	947.96a	142.84a
c_{gd}	49.91a	55.86a	159.65a	72.53a	413.13a	45.96a
CMOS DIFFERENTIAL AMPLIFIER AT 32nm (DC analysis)						
MODEL	NMOS-1	NMOS-2	PMOS-3	PMOS-4	NMOS-5	NMOS-6
REGION	SAT	SAT	SAT	SAT	SAT	SAT
i_d	11.60u	8.44u	-11.60u	-8.87u	20.05u	10.00u
V_{gs}	618.43m	618.43m	-647.36m	-647.36m	676.60m	676.60m
V_{ds}	1.17	919.41m	-647.36m	-906.77m	73.81m	676.60m
V_{th}	524.70m	548.00m	-513.25m	-485.99m	623.96m	569.81m
V_{dsat}	111.80m	99.96m	-146.15m	-165.56m	92.48m	120.10m
beta	2.34m	2.29m	1.20m	664.85u	8.77m	1.72m
g_m	134.09u	110.95u	135.71u	88.55u	250.76u	109.02u
c_{gs}	144.11a	135.09a	298.94a	165.02a	532.52a	116.86a
c_{gd}	32.37a	37.33a	104.41a	40.59a	279.25a	40.23a
CMOS DIFFERENTIAL AMPLIFIER AT 22nm (DC analysis)						
MODEL	NMOS-1	NMOS-2	PMOS-3	PMOS-4	NMOS-5	NMOS-6
REGION	SAT	SAT	SAT	SAT	SAT	SAT
i_d	7.08u	4.4933u	-7.08u	-4.82u	11.58u	10.00u
V_{gs}	622.62m	622.62m	-659.63m	-659.63m	704.43m	704.43m
V_{ds}	1.04	838.68m	-659.63m	-866.91m	94.40m	704.43m
V_{th}	550.03m	577.49m	-534.39m	-503.76m	676.09m	595.27m
V_{dsat}	97.99m	85.00m	-140.96m	-164.52m	78.96m	119.09m
beta	1.95m	1.89m	832.29u	366.52u	7.07m	1.78m
g_m	92.45u	67.97u	92.49u	51.32u	182.16u	109.16u
c_{gs}	82.62a	74.46a	179.93a	79.20a	297.19a	90.26a
c_{gd}	20.71a	25.15a	66.20a	20.88a	182.92a	31.53a

2. TRANSIENT ANALYSIS:-

2.1 Input parameter

Technology	At 45nm	At 32nm	At 22nm
V_{in}	0.1v	0.1v	0.1v
R_L	100K	100K	100K
C_L	100f	100f	100f
V_{dd}	1.1V	0.95V	0.9V
V_{ss}	-1.1V	-0.95V	-0.9V
Iref	10u	10u	10u

2.2 Input-output voltage versus time curve

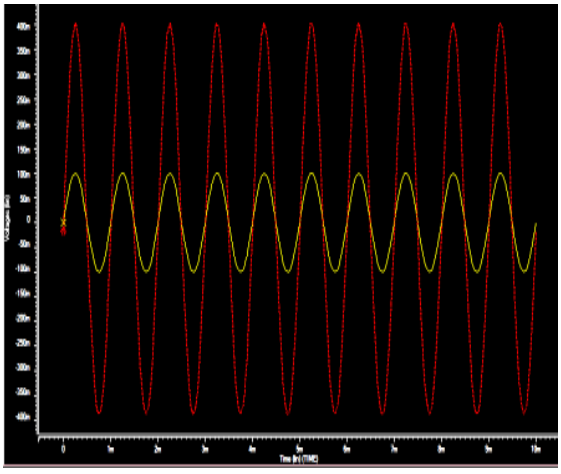

Fig.3.4 at 45nm

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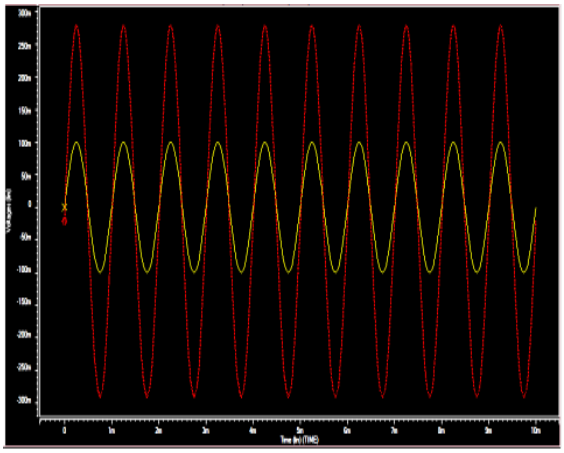

Fig.3.5 at 32nm

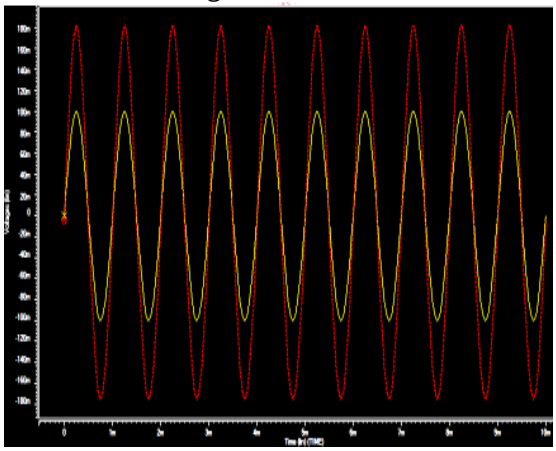

Fig.3.6 at 22nm

Where:-

Red indicate output voltage

Yellow indicate input voltage

Figure 3.4-3.6 shows the transient analysis for a sinusoidal input with peak-to-peak amplitude of 0.2V applied to the CMOS differential amplifier at a frequency of 1kHz. An output waveform is obtained at output port v(5); 0.8v, 0.57v and 0.35v at 45nm ,32nm and 22nm respectively.

2.3 Output parameter

Technology	At 45nm	At 32nm	At 22nm
Average power dissipation (uW)	127.02	67.303	37.39
Gain(db)	12.04	9.09	4.86
Output Voltage(volts)	0.8	0.57	0.35

2.4 Internal parameter

The various internal parameters mentioned in TABLE 1.2 are
Currents: **Id**.
Voltages: **Vgs, Vds, Vth, Vdsat.**
Transconductance: **gm**.
Capacitances: **Cgd, Cgs.**

Current gain: Beta.
various subscripts Indicates:
g for gate terminal
d for drain terminal
s for source terminal
th for threshold
sat for saturation

TABLE 1.2

CMOS TECHNOLOGY AT CHANNEL LENGTH 45nm (TRANSIENT ANALYSIS)						
MODEL	NMOS-1	NMOS-2	PMOS-3	PMOS-4	NMOS-5	NMOS-6
REGION	SAT	SAT	SAT	SAT	SAT	SAT
i_d	30.02u	24.49u	-30.02u	-24.31u	54.52u	10.00u
V_{gs}	743.25m	743.25m	-746.88m	-746.88m	703.38m	703.38m
V_{ds}	1.09	724.94m	-746.88m	-1.11	356.74m	703.38m
V_{th}	555.44m	578.49m	-533.80m	-506.99m	601.34m	579.83m
V_{dsat}	159.10m	147.38m	-195.28m	-211.34m	114.62m	125.09m
beta	2.43m	2.39m	1.47m	965.21u	9.95m	1.42m
g_m	206.53u	189.80u	214.07u	152.36u	582.43u	95.78u
c_{gs}	259.38a	256.11a	513.18a	333.24a	982.05a	142.84a
c_{gd}	55.43a	80.13a	158.88a	70.74a	397.86a	45.96a
CMOS TECHNOLOGY AT CHANNEL LENGTH 32nm (TRANSIENT ANALYSIS)						
MODEL	NMOS-1	NMOS-2	PMOS-3	PMOS-4	NMOS-5	NMOS-6
REGION	SAT	SAT	SAT	SAT	SAT	SAT
i_d	18.16u	13.70u	-18.16u	-13.48u	31.86u	10.00u
V_{gs}	685.12m	685.12m	685.48m	685.48m	676.60m	676.60m
V_{ds}	949.63m	663.59m	685.48m	971.53m	264.87m	676.60m
V_{th}	545.29m	570.98m	-509.24m	-479.19m	606.79m	569.81m
V_{dsat}	138.52m	124.38m	-177.09m	-198.60m	100.91m	120.10m
beta	2.22m	2.17m	1.20m	663.49u	8.90m	1.72m
g_m	164.21u	143.41u	169.16u	105.56u	422.36u	109.02u
c_{gs}	155.10a	150.42a	313.08a	171.06a	569.01a	116.86a
c_{gd}	37.04a	52.30a	103.29a	39.20a	270.03a	40.23a
CMOS TECHNOLOGY AT CHANNEL LENGTH 22nm (TRANSIENT ANALYSIS)						
MODEL	NMOS-1	NMOS-2	PMOS-3	PMOS-4	NMOS-5	NMOS-6
REGION	SAT	SAT	SAT	SAT	SAT	SAT
i_d	10.04u	6.72u	-10.04u	-6.67u	16.77u	10.00u
V_{gs}	676.23m	676.23m	-684.15m	-684.15m	704.43m	704.43m
V_{ds}	892.07m	671.05m	-684.15m	-905.17m	223.76m	704.43m
V_{th}	570.41m	599.69m	-530.76m	-498.11m	658.95m	595.27m
V_{dsat}	116.5m	101.07m	-163.01m	-188.70m	86.53m	119.09m
beta	1.85m	1.80m	835.05u	367.27u	7.20m	1.70m
g_m	110.54u	87.72u	112.11u	59.37u	256.10u	109.16u
c_{gs}	89.59a	83.95a	186.78a	81.40a	322.71a	90.26a
c_{gd}	23.67a	32.36a	65.46a	20.32a	178.50a	31.53a

3- AC ANALYSIS

3.1 Input parameter

Technology	At 45nm	At 32nm	At 22nm
V_{in}	0.1v	0.1v	0.1v
R_L	100K	100K	100K
C_L	100f	100f	100f
V_{dd}	1.1V	0.95V	0.9V
V_{ss}	-1.1V	-0.95V	-0.9V
Iref	10u	10u	10u

3.2 Differential gain, Phase & CMMR curve

For the frequency response plot, an AC signal of 0.1V is swept with 6 points per decade from a frequency of 10Hz to 1GHz. Fig.3.7-3.15 illustrates the frequency response which shows a AC gain in dB, phase in degree and CMMR versus frequency in Hz(in log scale)

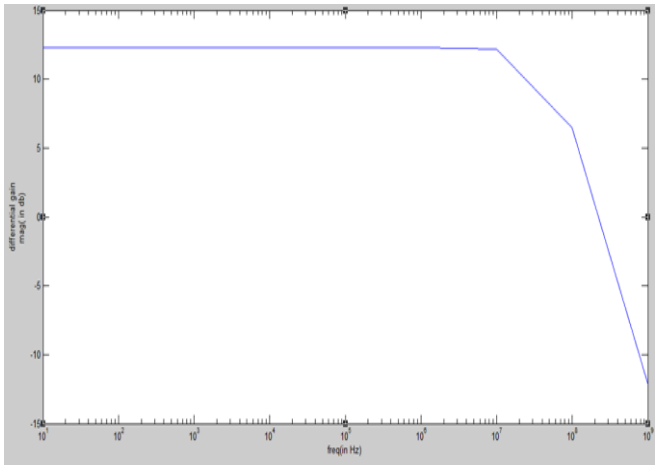

Fig.3.7 Differential gain at 45nm

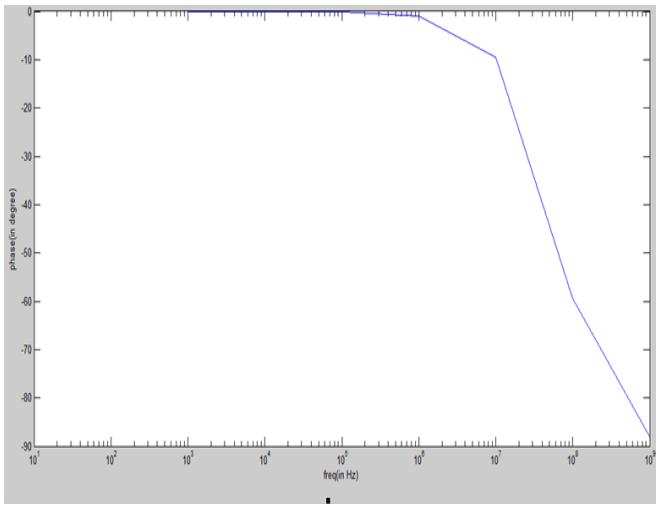

Fig.3.8 Differential phase at 45nm

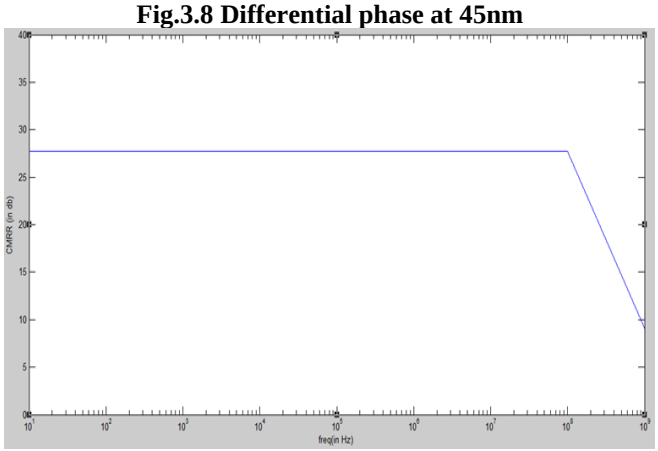

Fig.3.9 CMRR at 45nm

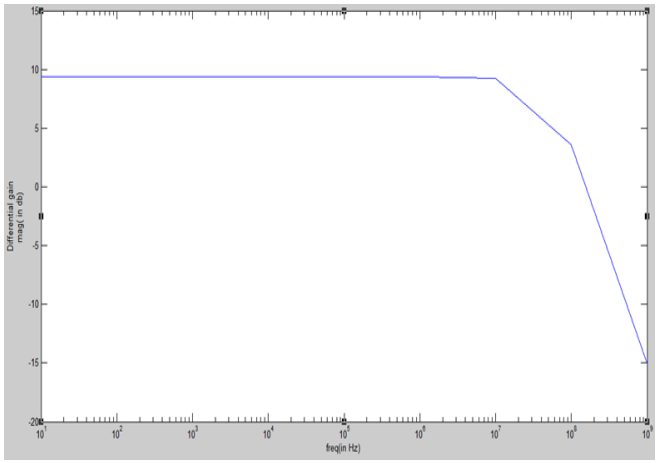

Fig.3.10 Differential gain at 32nm

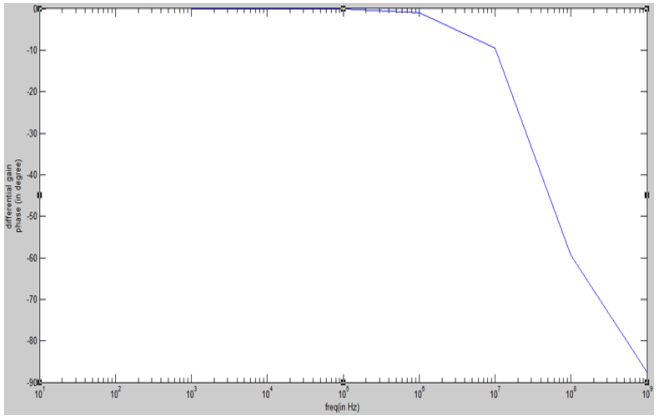

Fig.3.11 Phase at 32 nm

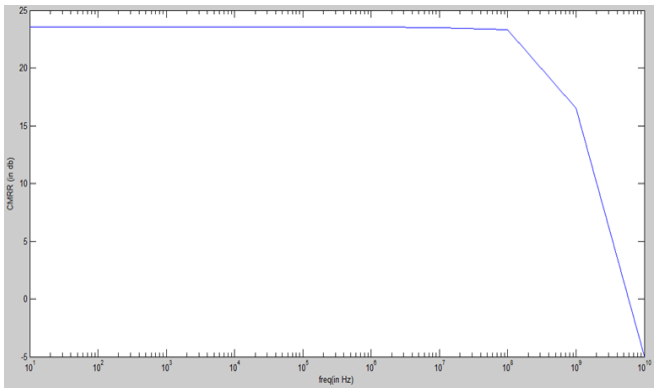

Fig.3.12 CMRR at 32 nm

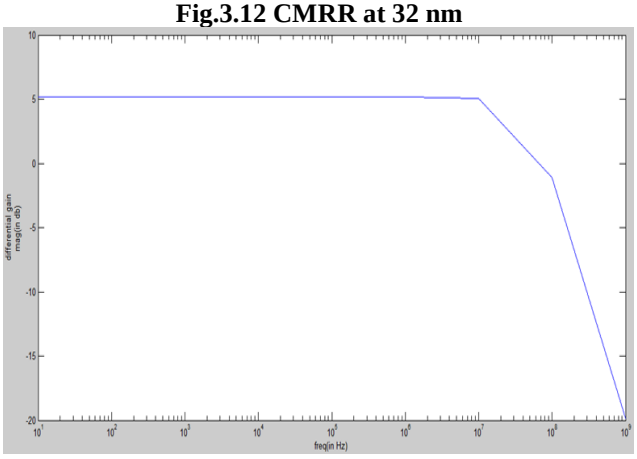

Fig 3.13 Differential gain at 22nm

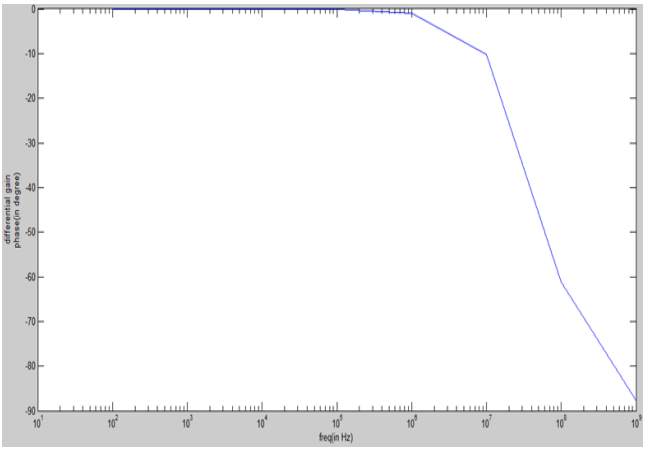

Fig 3.14 Phase at 22nm

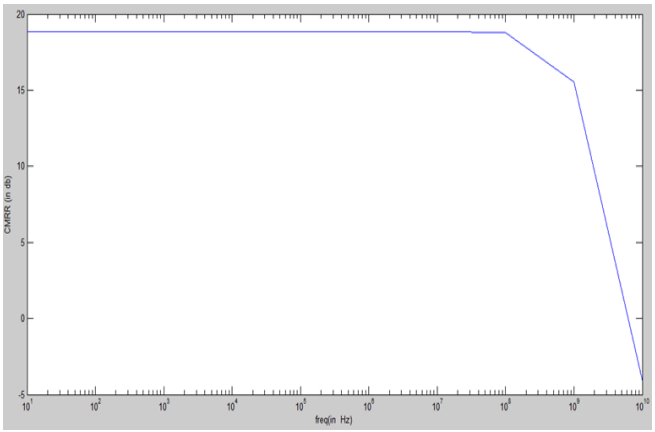

Fig.3.15 CMRR at 22nm

3.3 Internal parameter

The various internal parameters mentioned in TABLE 1.3are Currents: **Id**, Voltages: **Vgs, Vds, Vth, Vdsat.**Transconductance: **gm**.
Capacitances: **Cgd, Cgs.**Current gain: Beta.
various subscripts Indicates:

g for gate terminal,
d for drain terminal
s for source terminal,
th for threshold
sat for saturation

3.4 Output parameter

Table. 1.3

Technology	At 45nm	At 32nm	At 22nm
Gain (in db)	12.30	9.39	5.20
-3db frequency (Mhz)	59.43	59.29	55.08
Phase margin	103.71	109.68	123.23
CMRR	27.77	23.53	11.78
Unity gain BW (Mhz)	238.23	164.43	83.94
GBW (Mhz)	730.98	556.73	286.42

CMOS DIFFERENTIAL AMPLIFIER AT 45nm						
MODEL	NMOS-1	NMOS-2	PMOS-3	PMOS-4	NMOS-5	NMOS-6
REGION	SAT	SAT	SAT	SAT	SAT	SAT
i_{d}	30.02u	24.49u	-30.02u	-24.31u	54.52u	10.00u
v_{gs}	743.25m	743.25m	-746.88m	-746.88m	703.38m	703.38m
v_{ds}	1.09	724.94m	-746.88m	-1.11	356.74m	703.38m
v_{th}	555.44m	578.49m	-533.80m	-506.99m	601.34m	579.83m
v_{dsat}	159.10m	147.38m	195.28m	-211.34m	114.62m	125.09m
beta	2.43m	2.39m	1.47m	965.21u	9.95m	1.42m
g_m	206.53u	189.80u	214.07u	152.36u	582.43u	95.78u
c_{gs}	259.38a	256.11a	513.18a	333.24a	333.24a	142.84a
c_{gd}	55.43a	80.13a	158.88a	70.74a	397.86a	45.96a
CMOS DIFFERENTIAL AMPLIFIER AT 32nm						
MODEL	NMOS-1	NMOS-2	PMOS-3	PMOS-4	NMOS-5	NMOS-6
REGION	SAT	SAT	SAT	SAT	SAT	SAT
i_{d}	18.16u	13.70u	-18.16u	-13.48u	31.86u	10.00u
v_{gs}	685.12m	685.12m	-685.48m	-685.48m	676.60m	676.60m
v_{ds}	949.63m	663.99m	-685.48m	-971.53m	264.8m	676.60m.
v_{th}	545.29m	570.98m	-509.24m	-479.19m	-479.19m	569.81m
v_{dsat}	138.52m	124.38m	-177.09m	-198.60m	100.91m	120.10m
beta	2.22m	2.17m	1.20m	663.49u	8.90m	1.72m
g_m	164.21u	143.41u	169.16u	105.56u	422.36u	109.02u
c_{gs}	155.10a	150.42a	313.08a	171.06a	569.01a	116.86a
c_{gd}	37.04a	52.30a	103.29a	39.20a	270.03a	40.23a
CMOS DIFFERENTIAL AMPLIFIER AT 22nm						
MODEL	NMOS-1	NMOS-2	PMOS-3	PMOS-4	NMOS-5	NMOS-6
REGION	SAT	SAT	SAT	SAT	SAT	SAT
i_{d}	10.04u	6.72u	-10.04u	-6.67u	16.77u	10.00u
v_{gs}	676.23m	676.23m	-684.15m	-684.15m	704.43m	704.43m
v_{ds}	892.07m	671.05m	-684.15m	-905.17m	223.76m	704.4m
v_{th}	570.41m	599.69m	-530.76m	-498.11m	658.95m	595.27m
v_{dsat}	116.55m	101.07m	-163.01m	-188.70m	86.53m	119.09m
beta	1.85m	1.80m	835.05u	567.27u	7.20m	1.78m
g_m	110.54u	87.72u	112.11u	59.37u	256.10u	109.16u
c_{gs}	89.59a	83.95a	186.78a	81.40a	322.71a	90.26a
c_{gd}	23.67a	32.36a	65.46a	20.32a	178.50a	31.53a

IV. RESULTS & DISCUSSIONS

The figure 4.1 depicts the variation of average power dissipation (in uW), gain (in db), and bandwidth (in MHz) with respect to the channel length at 22nm, 32nm, and at 45nm respectively of the CMOS based differential amplifier. The graph clearly shows that as the channel length decrease in the sequence, 45 nm, 32 nm, & 22nm the average power dissipation decrease and bandwidth is maintained near about 55MHz while the gain of the differential amplifier is decreased as channel length is decreased in the sequence 45nm, 32nm and 22nm respectively.

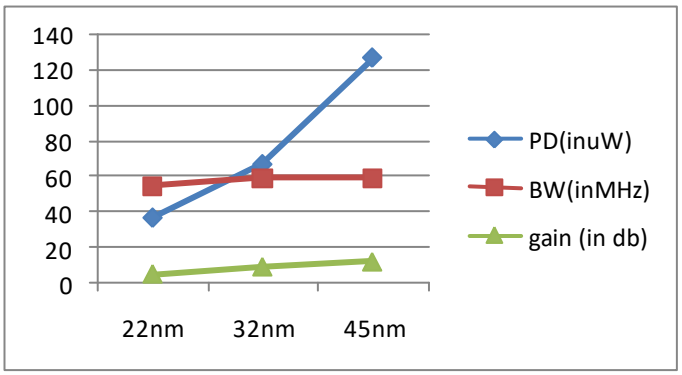

Figure.4.1

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Adil Zaidi has received his Bachelors Degree B.Tech in Electronics & Communication from CET-IILM-AHL, Greater Noida, and Master's Degree M-.Tech in VLSI Design from Maharishi Dayanand University, Haryana. His research interest includes Analog & Digital VLSI Design, Low Power Circuits, CNTFET, Nanoelectronics etc.Presently he is serving as Assistant Professor in the Department of Electronics and communication Engineering, CET-IILM-AHL, GreaterNoida Uttar Pradesh, India.

Divakar veer Vikram singh is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had done his summer training from B.H.E.L IP Jagdishpur, Sultanpur U.P.

Firoz is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had done his summer training from B.H.E.L IP Jagdishpur, Sultanpur U.P.

Dileep Kumar is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had done his summer training from B.H.E.L IP Jagdishpur, Sultanpur U.P.

Veerandra pratap is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had done his summer training from CETPA Noida U.P.