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Improving Accuracy in Mitchell's Logarithmic Multiplication using Iterative Multiplier for Image Processing Application

Deeksha R Shetty, Savitha Patil

Abstract*— *The logarithmic of a binary number may be determined approximately from the number itself by simple shifting and counting. Since the logarithms used are approximate there can be errors in the result. This paper presents a simple and efficient logarithmic multiplier with the possibility to achieve an arbitrary accuracy through an iterative procedure. Digital image processing is used in variety of application .Many algorithm used in image processing include convolution. In this coding is done using VHDL for the FPGA. Synthesis and simulation is done using Xilinx and MATLAB is used to convert input image in to a matrix form which is convolved with the kernel value using proposed multiplier and the result is again converted back into a image form using m.file.

Key word*— *logarithmic number system , computer arithmetic , digital signal processing, multiplier, convolution.

I. INTRODUCTION

Digital signal processing uses different arithmetic operations such as multiplication. In Multiplication, for large value operands it has always been hardware, time and power consuming arithmetic operation. In some signal processing application priority is given to the speed rather accuracy in that case logarithm number system for multiplication is suitable method. Whereas some application in which the result of arithmetic operation or in this case results of multiplication need not be exactly accurate.When accuracy is given more importancethan the speed iterative logarithmic multiplier is more suitable method.

Multiplication using logarithms there are two methods[1].one using lookup table and the other based on Mitchell's algorithm that computes thelogarithms through shift and count operation. lookup table based logarithmic multiplication uses complete tables of logarithm values stored in memory hence for this memory required is more. Mitchells algorithm doesnot require a memory but there is loss of accuracy[2] .The proposed multiplier improve the accuracy in Mitchells algorithm.LNS based multiplication methods are categorised in to two methods.One is the method that use lookup tables and interpolation and second based on Mitchell's algorithm that computes the algorithm through shift and count operations[1] .The advantage of Mitchell's algorithm over look table method is it doesn't require memory .But there is a disadvantage in Mitchell which is loss of accuracy. Thus, several methods are proposed to improve the accuracy in Mitchell's algorithm.

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II. BINARY LOGARITHMS

One of the most significant multiplication methods in logarithm number system is Mitchell's algorithm. In MA two operands are multiplied by finding their logarithm, adding them and taking the antilogarithm of the sum.

The number N can be written as [2] ,

$$N = \sum_{i=j}^{k} 2^i * z_i \qquad (1)$$

Where z_i =0,1. Since z_k is the most significant bit.

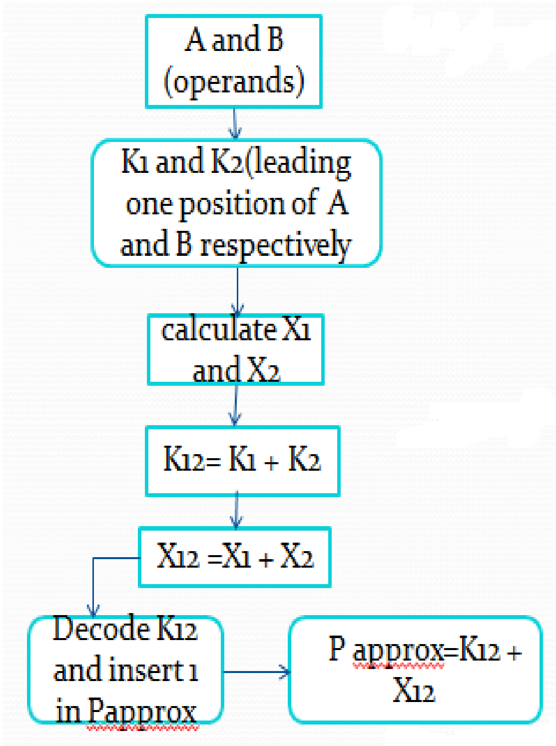

Figure 1 : Mitchell's based algorithm

Approximation of the logarithm and antilogarithm is derived from binary representation of numbers.

$$N = 2^k \left(1 + \sum_{i=j}^{k-1} 2^{i-k} * z_i\right)$$

$$N = 2^k (1 + x) \qquad (2)$$

Where k is the characteristic number or place of the most significant bit with the value of 1,Zi is the bit value at i^{th} position is the fraction depends on the number precision.

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MA produces an significant error .this error increases with the number of bits with the value of 1' in the mantissa.The MA based multiplication algorithm is given [2].

III. PROPOSED MULTIPLIER

In this approach Iterative procedure is applied to the Mitchells algorithm for logarithmic multiplication.The proposed multiplier avoids logarithm approximation and introduces an iterative algorithm with various possibilities for minimizing the error and produce the exact result In this number of iteration for exact result depends on the number of bits with the value of '1' in the operand with a smaller number of bits with the value of '1'.

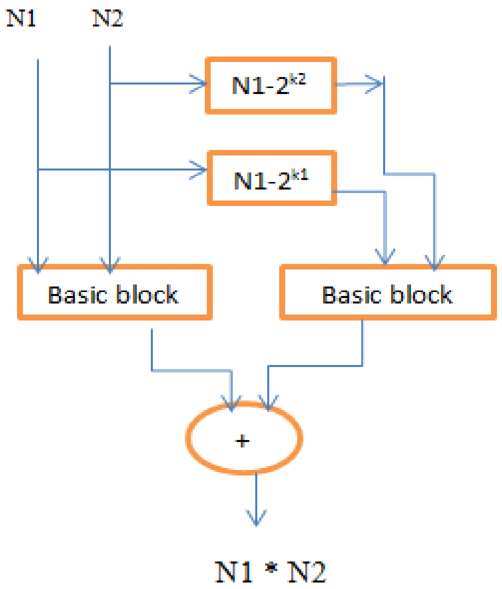

Figure 2 : Basic block

The multiplier is composed of two basic blocks of which the first calculates the approximate product while second one calculates the error correction term. .

IV. HARDWARE IMPLEMENTATION

To evaluate the performance of the proposed multiplier we implementing it on FPGA using Xilinx 8.2i. Coding is done using VHDL[8] , which stands for Very High Speed Integrated Circuit Hardware Description Language for the FPGA. Synthesis and simulation is done using Xilinx.

APPLICATION OF PROPOSED MULTIPLIER IN IMAGE PROCESSING

Convolution is one of the main computations in digital signal processing .In this paper Convolution process is used to multiply the pixel values of the image with the kernel value. Each pixel values multiplied with the kernel value[3] .In Gaussian filter the image is convolved with Gaussian kernel values to eliminate high frequency components .The 2-D zero mean Gaussian function is given in equation[3] and is sampled truncated to obtain 3x3 Gaussian kernels as shown in figure (3).

$$G(x,y)=\frac{1}{2\pi\sigma^2}e^{-\frac{(x^2+y^2)}{2\sigma^2}} \qquad (3)$$

$$\frac{1}{256}*\begin{bmatrix}21 & 31 & 21\\ 31 & 48 & 31\\ 21 & 31 & 21\end{bmatrix}$$

Figure 3: Gaussian 3x3 Kernel

The 3x3 matrix is considered from the input image and convolved with 3x3 Gaussian Kernel window . using an equation(4). The convolution process is continued for entire image by shifting one column every time.

$$y(m,n)=\sum_{i=1}^{rows}\sum_{j=1}^{columns} h(i,j).x(m-i,n-j) \qquad (4)$$

Where x is the input image
h is the filter mask
y is the output image
rows is the number of rows in input image
columns is number of columns in input image.

The MATLAB algorithm performs the convolution between the matrix which is converted from image to matrix form and the kernel value .Size of the input pixel window is always same as the convolutional mask.

Convolutional algorithm is shown in Figure [4] with an input pixel window ,the convolutional mask and the resulting output .Output pixel value is rounded to the nearest value.

$$\begin{bmatrix}X1 & X2 & X3\\ X4 & X5 & X6\\ X7 & X8 & X9\end{bmatrix}*\begin{bmatrix}Y1 & Y2 & Y3\\ Y4 & Y5 & Y6\\ Y7 & Y8 & Y9\end{bmatrix}\rightarrow\begin{bmatrix} & & \\ & P & \\ & & \end{bmatrix}$$

Figure 4 : convolution

V. VHDL AND MATLAB

In order to simulate real image data in VHDL it is important to create a method of transferring image to a matrix form. MATLAB is used to do this functionality which is quite efficient in manipulating matrix data .MATLAB m-file is created to take an input file in the bitmap format and convert it to a file with a new word of data on every line .Data in this format will be read in to the VHDL test bench by using standard VHDL text input/output function[8]. After simulating this data ,the output data of the algorithm is written by the test bench into another file. One more MATLAB m-file is used to read that data and convert it back into a matrix form.

VI. RESULT AND CONCLUSION

In this paper the proposed multiplier improve the accuracy of the Mitchell algorithm based logarithm multiplication using iterative procedure .This approach improves the error percentage compared to the basic Mitchell algorithm multiplication. By using only three correction terms the error of any multiplication result is less than a 0.5%.MATLAB is used to convert input image in to a matrix form which is convolved with the kernel value proposed multiplier and the result is again converted back into a image form using m.file and PSNR value will be displayed of original image and the output image.

The PSNR values of corrupted image with noise and smoothened images are tabulated as shown below for scaling factor of Gaussian kernels 256.

Table 1 : PSNR values

Type of multiplier	PSNR of corrupt image(dB)	PSNR of smoothened image(dB)
MA based multiplier	14.4782	16.5914
Iterative multiplier	14.4782	18.4884

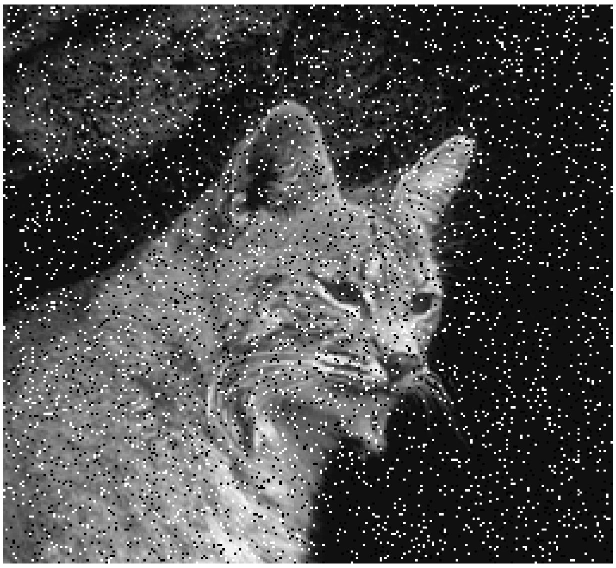

Figure 5 : Input image

Figure 6: Image using MA based multiplier

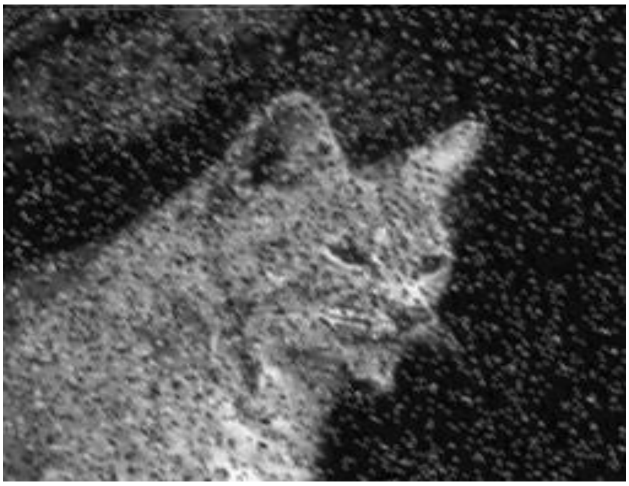

Figure 7: Image using proposed multiplier

Table 2: Device utilization of proposed multiplier

Number of Slices	233 out of 1331	1%
Number of Slice flip flops	62 out of 26624	0%
Number of 4 input LUTs	423 out of 26624	1%
Number of IOs	33	
Number of bonded IOBs	33 out of 221	14%
Number of GCLKs	1 out of 8	12%

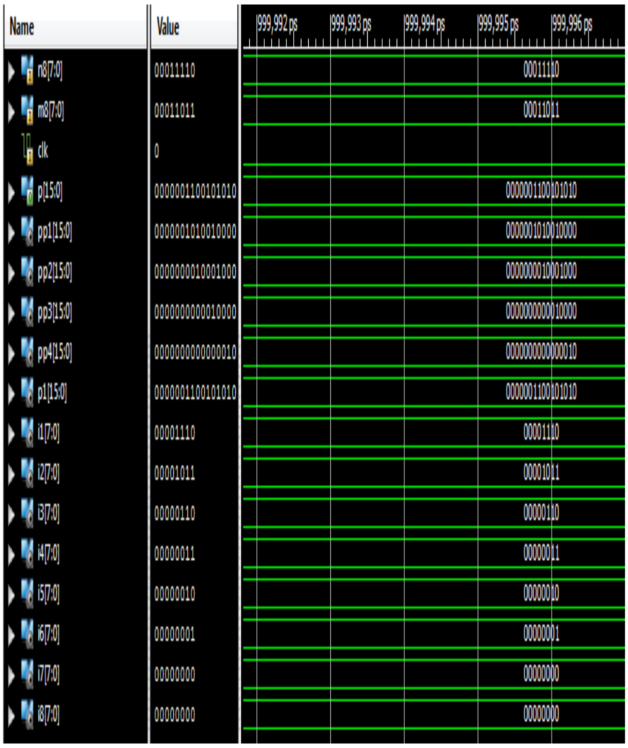

Figure 8 : Simulation Result

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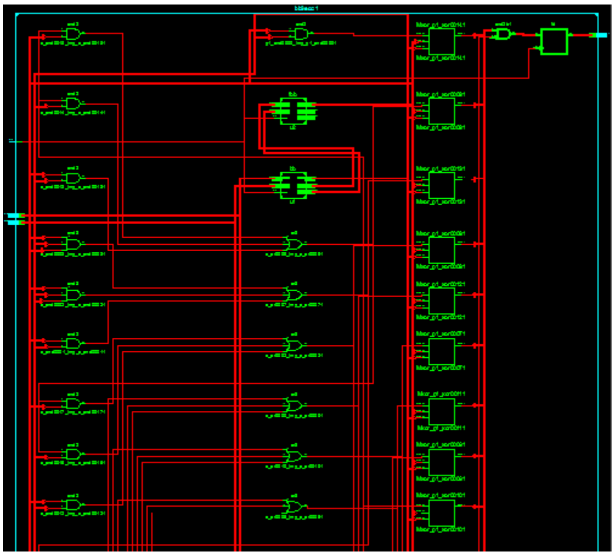

Figure 9 : RTL Schematic

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