Design of D Flip-Flip Using Nano-Technology based Quantum Cellular Automata

Tamal Sarkar

Abstract*—Lot of research has been going on for implementing digital systems at nano-scale level. Quantum-dot based Quantum Cellular Automata (QCA) is a promising as well as emerging technology for implementing of digital systems at nano-scale. By taking full advantage of the unique feature of this technology, it is possible to have device which functions consuming ultra low power and very high operating speeds. In this work, we have selected few basic flip-flops and studied them well. Using the computational tools "QCADesigner" proposed for designing QCA based digital circuits; we have designed the QCA circuits of D-Flip Flop. The correctness of the proposed circuits is also verified using simulation results obtained using QCADesigner.

***Index Terms*— Quantum Dot, QCA, Nano-electronic circuit, Binary logic, D-Flip Flop, Cell-Cell Response.**

I. INTRODUCTION

The current idea of Quantum dot developed from the concept of artificial semiconductor atoms [1, 2]. In 1992, Meurer and his group demonstrated that it is possible to have controllable occupation of these quantum dots in the few-electron regime. As such, we may have '*quantum-dot hydrogen'*, '*quantum-dot helium'*, '*quantum-dot lithium'* and '*quantum-dot molecules'*. In quantum-dot molecules, there exist coupling between quantum-dot atoms in close proximity [3]. Quantum-dot cellular automata (QCA) are locally interconnected cellular-automata-like arrays of nanostructures (quantum dots). Here interconnections are given by the physical interactions. The underlying physics determines the overall functioning of such arrays [4]. The QCA approach adopts an approach to code information as to eliminate the most of the problems associated with current-switching paradigm for nano-devices. The QCA scheme is not a quantum computer as they do not require quantum mechanical phase coherence over the entire array. Phase coherence is only required inside each cell whereas cell-cell interactions are classical. This makes QCAs a more attractive candidate for circuit design. The QCA scheme consisted of four quantum dots [5, 6] are very popular and are schematically shown in Fig.1.In this scheme, the electrons jumps between the individual quantum dots cell through quantum mechanical tunneling [7,8]. The electrons also experience coulomb repulsion but are constrained to occupy the dots. If they are left alone, they may have two basic configurations. Based on the alignment of the charge, we may associate a polarization as in Fig. 1. Again, it is to be noted that the ground state of an isolated cell has a net polarization of zero.

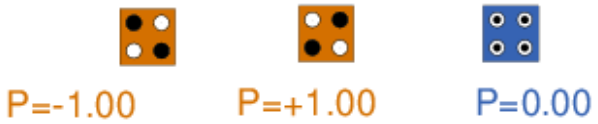


Figure 1 QCA Cell

This paper is organized as follows. In section II, an introduction to basic logic primitive effectively required to design QCA based circuit were introduced. Section III gives a very brief review of Latches and Flip Flops. Section IV uniquely describes characteristic equation, characteristic table and excitation table of a D-Flip-Flop whereas section V describes design methodology and design verification of D Flip-Flop. Finally, we conclude this paper in Section VI.

II. BASIC QCA GATES

Logic units are the basic building blocks of many computational operations like arithmetic, multiplexer, de-multiplexer, radix conversion, parity generator cum checker etc. The combination of basic gates like AND, OR, NOT as well as NAND or NOR are universal gate. The combination of these gates logic is considered universal because any general Boolean function can be implemented with a combination of logic primitive.

In case of computing with QCA, we also require such universal logic primitive. One such logic primitive that may be created with QCA is a Majority Voter (MV) gate, which is shown in the Fig. 2. The truth table of the operation is also shown in the TABLE I. The logic function of a MV gate [9-12] is

$$MV(A,B,C) = AB + BC + CA \tag{1}$$

If C = -1.00 polarized i.e. logic level '0' then, MV (A, B, 0) = AB = AND gate.
Also if C = +1.00 polarized i.e. logic level '1' then, MV (A, B, 1) = AB+B+A = A+B = OR gate.

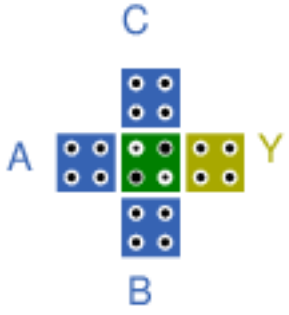


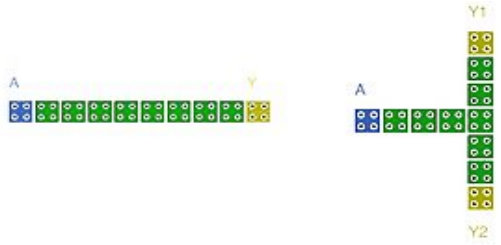
Figure 2 QCA based Majority Voter (MV) gate

Manuscript received September, 2013.
Tamal Sarkar, University Science Instrumentation Centre, University of North Bengal, Siliguri, India.

TABLE I: Truth Table of MV gate

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Using a line of QCA cells, we can have a binary wire Fig. 3(a). 'FANOUT' means one signal comes in and several copies go out. The fan out of QCA is very high as there is negligible power requirement for any type of gate in this technology. The information pumps down in circuit in a controllable manner. The implementation of 'FANOUT' using QCA is shown in Fig. 3(b)



(a) (b)

Figure 3 (a) QCA based binary wire (b) FANOUT

III. A REVIEW OF LATCHES AND FLIP-FLOPS

Latches and Flip Flops (FFs) circuit can maintain a binary state indefinitely directed by an input signal to switch states subject to the condition that as the power is delivered. There are a wide variety of latches and FFs. They differ from each in terms of number of inputs and how these inputs affect the binary state. The main difference between latches and FFs is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. But, in FFs, the content changes only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the FF content remains constant even if the input changes. There are basically four main types [13] of latches and FFs: *SR, D, JK and T* as shown in Fig. 4. Each type can have different variations such as active high or low inputs, whether they change state at the rising or falling edge of the clock signal, and whether they have asynchronous inputs or not. The FFs can be described fully and uniquely by its logic symbol, characteristic table, characteristic equation, excitation table.

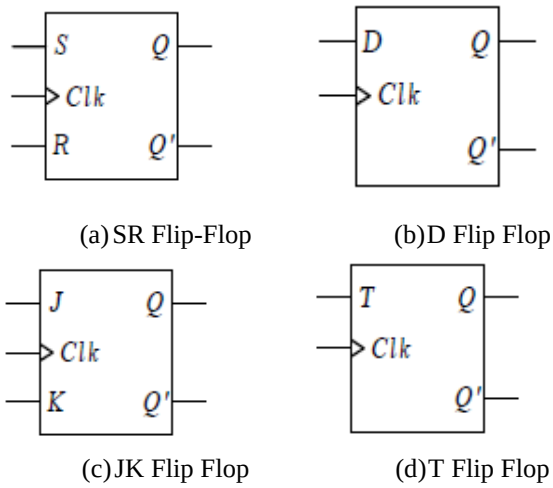
Logic symbol of FFs describes the FF's inputs and outputs, the name given to these signals, and whether they are active high or low. All the FFs have Q and Q` as their outputs. All of them also have a clock input. The small triangle at the clock input indicates that the circuit is a FF and so it is triggered by the edge of the clock signal; if there is a circle in front, then it is the falling edge, otherwise, it is the rising edge of the clock signal. Without the small triangle, the circuit is a latch.

Truth table is simply lists all possible combinations of the input signals, the current state (or content) of the FF, and the next state that the FF will go to at the next active edge of the clock signal.

Characteristic table is just the truth table but usually written in a shorter format. The characteristic table answers the question of what is the next state when given the inputs and the current state, and is used in the analysis of sequential circuits.

Characteristic equation is the fundamental Boolean equation that is derived from the characteristic table. This equation formally describes the functional behavior of the FF. Like the characteristic table, it specifies the FF's next state as a function of its current state and inputs.

Excitation table gives the value of the FF's inputs that are necessary to change the FF's current state to the desired next state at the next active edge of the clock signal. This table give answers to the question regarding what should be the inputs when given so that the current state that the FF is in and the next state that we want the FF to go to. This table is used in the synthesis of sequential circuits.



(a) SR Flip-Flop (b) D Flip Flop

(c) JK Flip Flop (d) T Flip Flop

Figure 4 Four main types of Flip Flops

IV. D FLIP-FLOP

D FF has single input D (data), D 'HIGH' is a SET state, D 'LOW' is a RESET state. Q follows D at the clock edge. A SR flip-flop can be converted into a D flip-flop by adding an inverter as shown in figure 5.

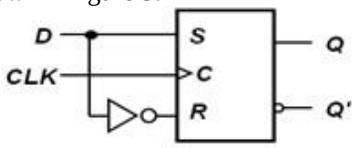


Figure 5 D- Flip-Flop from SR Flip-Flop

Characteristic Equations of D Flip Flop is

$$Q_{DFF} = DQ'_{t-1} + DQ_{t-1} \quad (2)$$

The characteristic table and excitation table for characteristic equation of D Flip-Flop is shown in the TABLE II and TABLE III respectively.

TABLE II: Characteristic table of D Flip-Flop

D	Q	Q_{next}
0	X	0
1	X	1

TABLE III: Excitation table of D Flip Flop

Q	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

V. DESIGN METHODOLOGY OF D-FLIP FLOP AND VERIFICATION USING QCA-DESIGNER

To design latch / FFs as mentioned earlier in section III, the conventional CMOS circuits are not suitable to direct translated into QCA architecture due to the timing constraint. By observing the truth tables as well as Boolean equations derived out of it, one may obtained the required variable as well as number of logic gates that may be required to design a particular latch or FF.

From section IV, we find that we can design a D FF using SR-Flip-Flop just by introducing inverter i.e. R will be an inverted input of S. The characteristic equation of D FF suggest that we need two AND gate and one OR to design a D FF. Using the concept of logic primitives of QCA design as discussed in section II, we can logically obtain the corresponding design equation using MV gate. QCA based design is requires one majority voter gates and the design equation is Q=M (D, Q, Q') = DQ+DQ' since QQ'=0. Authors of Huang et al. [14] indicated that D FFs can be implemented using binary wires in a QCA where input signal is delivered in to the output after at least one clock cycle delay. Although this is acceptable regarding the clocking phases in QCA data flow, but timing constraint and synchronization of components must be considered due to the fact that the four-phase clock signal also control the combinational gates [15]. So, we have to introduce independent clock input with optimized delay and proper cell utilization. This reduces the effects of timing constraints.

A. QCA design of D-Latch and D-FF

The D- Latch is constructed from 29 cells whereas D-FF is constructed from 43 cells. The D-Latch and D-FF has been simulated using 'QCADesigner' which is a layout as well as simulation tool for QCA design. The Fig. 6 and Fig. 7 respectively shows the QCA based proposed design of a D-Flip-Flop without clock (Latch) and D-Flip-Flop with clock. The designs essentially require multi-phased clocking mechanism with proper information flow. The different colors in the design indicate different clocking zones.

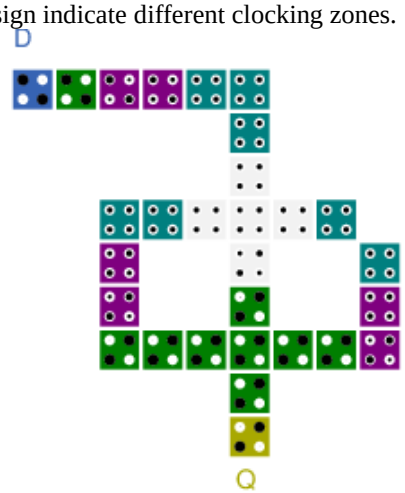


Figure 6 D Latch

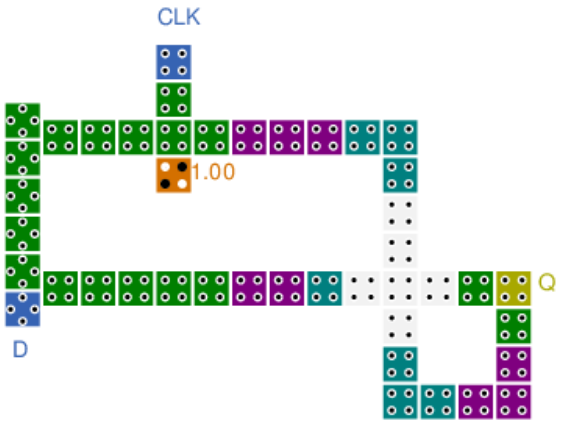


Figure 7 D-Flip-Flop

B. Design Verification

Each of circuit as given in Fig.6 and Fig.7 were tested with "QCADesigner ver. 2.0.3". Bi-stable approximation is done with default values i.e. Number of samples: 12800, Radius of effect: 65 nm, Clock high: 9.8e-22, Clock Low: 3.8e-22, relative permittivity of 12.9, Upper Threshold: 0.5, Lower Threshold: -0.5, Cell size: 18 nm. From Excitation Table of D FF, we note that D=1, Q=X, Q_{next}=1. The same is verified as in figure 8 and 9.

The expected time trace of the D latch for excitation starting with Q=1 will be equivalent to TABLE IV and expected for Q=0 will be equivalent to TABLE V

TABLE IV: Truth table of D Latch with initial value of Q=1

D	$Q_t = DQ'_{t-1} + DQ_{t-1}$
0	1 (initial value)
1	0
0	1
1	0
0	1
1	0
0	1
1	0

TABLE V: Truth table of D Latch with initial value of Q=0

D	$Q_t = DQ'_{t-1} + DQ_{t-1}$
0	0 (initial value)
1	0
0	1
1	0
0	1
1	0
0	1
1	0

The simulation results for D latch for Q=1 (initial) as shown in Fig. 8 and for Q=0 (initial) as in Fig. 9 has been obtained by simulating the QCA layout. From the simulation waveforms it can be seen that the timing trace of the D latch for Q=1 and Q=0 initial value matches with the

theoretical values as given in TABLE IV and TABLE V.

TABLE VI: Truth table of D FF with initial value Q(t-1)=1

D	CLOCK	Q (t)
0	0	**1**
0	1	**1**
1	0	**1**
1	1	**0**
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**0**

Similarly, the expected time trace of the D FF for excitation starting with Q=1(initial value) will be equivalent to TABLE VI and expected for Q=0 (initial value) will be equivalent to TABLE VII. The simulation results for D FF for Q=1 (initial) as shown in Fig. 10 and for Q=0 (initial) as in Fig. 11 has been obtained by simulating the QCA layout. From the simulation waveforms it can be seen that the timing trace of the RS flip-flop for Q=1 and Q=0 initial value matches with the theoretical values as given in TABLE VI and TABLE VII.

TABLE VII: Truth table of D FF with initial value Q(t-1)=0

D	CLOCK	Q (t)
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**0**
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**0**

C. Output Parameter obtained from Simulation

For D-Latch, it is seen that the polarization at the output is '$\pm 9.51e^{-001}$' (for both Q and Q') for bi-stable approximation as well as coherence vector options with Euler method. If we take temperature 5 k instead of default value of 1K in coherence vector option keeping the method same, the corresponding value of polarization is '$\pm 9.\ 50e^{-001}$' (for Q'). But the further increase in step of 1 K i.e. at 6K, the circuit fails to provide any good result.

For D-FF, it is seen that the polarization at the output is '$\pm 9.87e^{-001}$' for bi-stable approximation as well as coherence vector options with Euler method. But, if we take temperature 6k or 7k instead of default value of 1K in coherence vector option keeping the method same, the corresponding value of polarization is remains same i.e.'$\pm 9.\ 87e^{-001}$'. Whereas, the further increase in step of 1 K i.e. at 8K, the circuit fails to provide any good result.

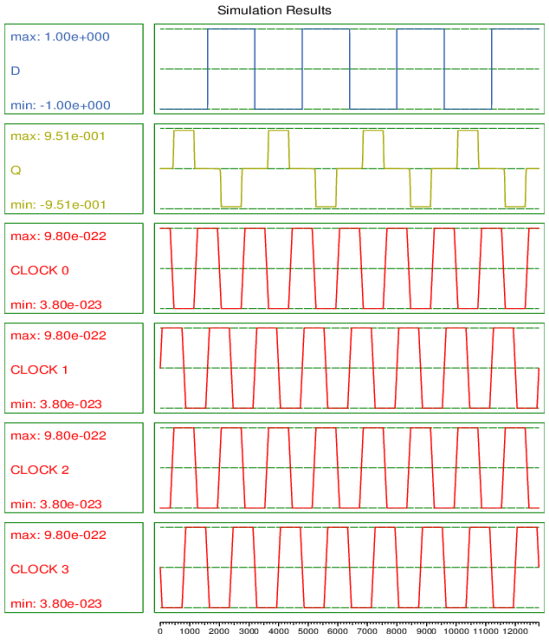


Figure 8 D-Latch (Cell-Cell Response for Q=1)

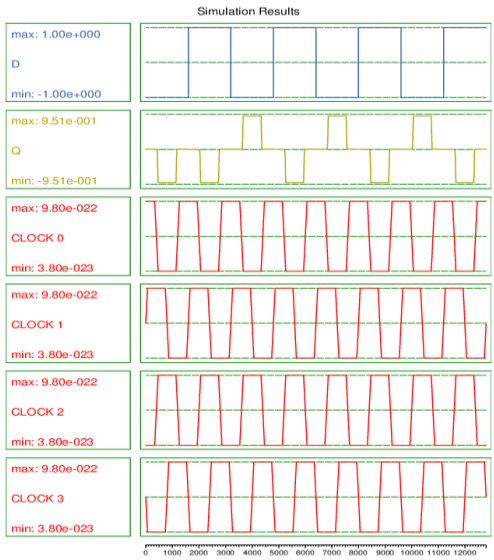


Figure 9 D-Latch (Cell-Cell Response for Q=0)

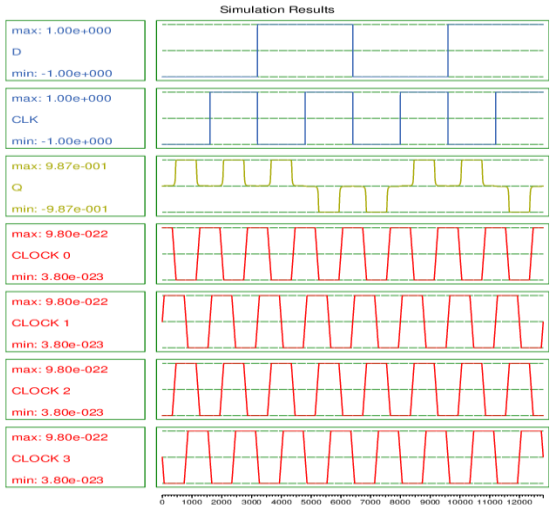


Figure 10 D Flip-Flop (Cell-Cell Response for Q=1)

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

VI. CONCLUSION

In this paper a conception of design methodology as well as comprehensive testing scheme for proposed design of D latch and D FF has been discussed. The proposed designs have efficient structures in terms of area, delay and cell count. Simulations of the proposed designs of D-latch and D-FF were carried out using both bi-stable and coherence engines (with different operating temperatures) of QCADesigner. For results verification, we have obtained the theoretical values of timing trace in tabular form (Truth Table) and minutely verified whether all the values match with the simulation waveforms. The logical structures thus designed, may be used as basic building block of a general purpose nano-computers/processors which may be a future technical advancement of current researches. Further, we like to conclude that the proposed designs as well as verification methodology will significant help in future work.

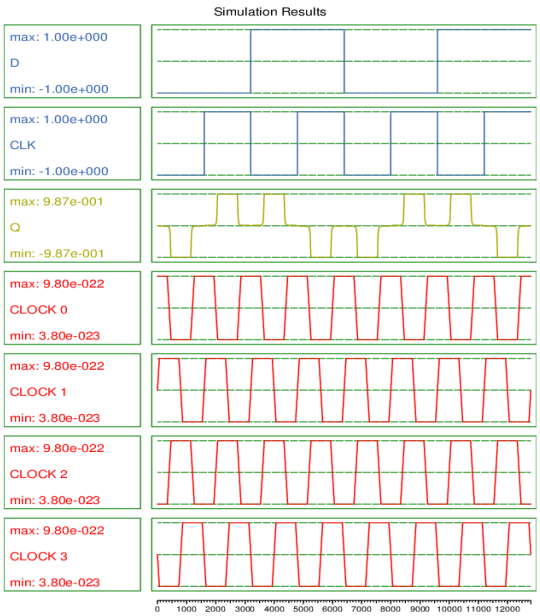


Figure 11 D Flip-Flop (Cell-Cell Response for Q=0)

ACKNOWLEDGMENT

The author acknowledges Dr. Tanay Chattopadhyay of WBPDCL for introducing him to the software 'QCADesigner' and Dr M.K. Das, Head, USIC, University of North Bengal for providing excellent research environment and facilities.

REFERENCES

[1] M. A. Reed, J. N. Randall, R. J. Aggarwal, R. J. Matyi, T. M. Moore, and A. E. Wetsel, "Observation of discrete electronic states in a zero-dimensional semiconductor nanostructure", *Phys. Rev. Lett.* vol. ***60***, 1988, pp. 535-539.

[2] U. Meirav, and M. A. Kastner, and S. J Wind, , "Single-electron charging and periodic conductance resonances in GaAs nanostructures", Phys. Rev. Lett. ,Vol. 65 (6), 1990, pp. 771—774, doi. 10.1103/PhysRevLett.65.771

[3] F. Hofmann, T. Heinzel, D.A. Wharam, and J.p. Kotthaus, "Single electron switching in a parallel quantum dot", Physical Review B,, vol. 51(19), 1995, pp. 13872-13875

[4] W. Porod, C. Lent, G. H. Bernstein, A. O. Orlov, I. Hamlani, G. L. Snider & J. L. Merz, "Quantum-dot cellular automata: computing with coupled quantum dots", vol. 86(5), 1999, pp. 549-590

[5] C. S. Lent, P D Tougaw, W. Porod and G. H. Bernstein, "Quantum cellular automata", vol. 4(1), 1993, pp.49-57

[6] C. S. Lent and P. D. Tougaw, "A device architecture for computing with Quantum dots", Proc. IEEE,vol. 85(4), 1997, pp.541-557

[7] T. Sarkar, S.C.Das and T.Chattopadhyay "Transition from MOSFET to Quantum Dot: An Overview", *International conference on fundamental & applications of nanoscience & technology, (ICFANT-2010), Jadavpur University*, Dec 9-11, 2010, pp.183-186.

[8] T.Sarkar, S.C.Das and T.Chattopadhyay, "Mathematical Modeling of Quantum Dot", *International Conference On Laser, Materials Science And Communication (ICLMSC-2011)*, University of Burdwan, December 07 to 09, 2011, 183-186, ISBN: 93-80813-14-7.

[9] K. Das and D. De, "Characterization, test and logic synthesis of novel conservative and reversible logic gates for QCA", International Journal of Nanoscience,vol. 9(3), 2010, pp.201-214

[10] I. Amlani, A. O. Orlov, G. Toth, G. H. Bernstein, C. S. Lent and G. L. Snider, "Digital logic gate using quantum-dot cellular automata", *Science*, vol. 284 (9), 1999, pp.289-291

[11] K. Das and D. De, "Characterization, applicability and defect analysis for tiles nanostructure of quantum dot cellular automata", *Molecular Simulation*, vol.37(3), 2011, pp. 210-225.

[12] Lee Ai Lim, Azrul Ghazali, Sarah Chan Tji Yan, Chien Fat, "Sequential circuit using Quantum-Dot Cellular Automata (QCA)", 978-1-4673-3119-7, Vol. 12,IEEE, 2012, pp. 162-167

[13] M. Morris Mano, Digital Logic and Computer Design, N.J., USA: Prentice –Hall .(Indian edition, published by Prentice-Hall of India Private Limited, Twenty-first Printing), 2000, pp. 204-233

[14] J. Huang, M. Momenzadeh, F. Lombardi, "Design of sequential circuits by quantum-dot cellular automata, Microelectronic .J. 38, 2007, pp. 426-429

[15] A.S. Shamsabadi, B.S. Ghahfarokhi, K. Zamianifar, N. Movahedinia, "Applying inherent capabilities of quantum-dot cellular automata to design D flip-flop case study", Journal of Systems Architecture, 55, 2009, pp. 180-187

Tamal Sarkar was born in Balurghat, West Bengal, India on September, 18, 1977. He received Bachelor Degree with Physics Honors in 1998 with first division from North Bengal University and Master Degree (Physics) in year 2000 with first division.

He is associated with University Science Instrumentation Centre, North Bengal University as Technical Officer (Grade-I) since 2007. His area of interest includes General Theory of Relativity, X-Ray Astronomy, Quantum Computing and Theoretical Opto-electronics. He has published five research articles in National and International Journals in above mentioned field. Apart from it, he is a guest faculty for the course of Post Graduate Diploma in Remote Sensing and GIS of Centre of Remote Sensing, North Bengal University. He has also worked as member of Expert Committees/ Tender Committees for University of North Bengal. He is also a member of FOSET, Kolkata.

.