A New Topology for Power Factor Correction using Resonant Converters

V V Vijetha Inti, Karthika Mangamuri, Ch Phani Kumar

Abstract ***—A new parallel-connected power flow technique is proposed to improve the input power factor with simultaneously output voltage regulation taking consideration of current harmonic standards. Paralleling of converter modules is used in medium-power applications to achieve the desired output power by using smaller size of high frequency transformers. A parallel-connected interleaved structure offers smaller passive components with less loss in continuous conduction inductor current mode and also reduces the volt-ampere rating of resonant (DC/DC) converter. MATLAB/SIMULINK is used for implementation and simulation results show the performance improvement.***

Keywords: Power Factor Correction (PFC), Total Harmonic Distortion, Forward converter, Flyback converter, Parallel Operation

I. INTRODUCTION

Most electronic equipment is supplied by 50-60 Hz utility power, and more than 50% of this power is processed through some kind of power converter. Generally power converters use a diode rectifier followed by a bulk capacitor to convert AC voltage to DC voltage. So these power converters absorb energy from the AC line only when the line voltage is higher than the DC bus voltage, the input line current contains rich harmonics, which pollute the power system and interfere with other electric equipment. These converters have a low power factor of 0.65. Because the conventional simple diode rectifier followed by a bulk capacitor cannot meet the requirements, which have stimulated the research of power factor correction techniques.

The objective of the project has been in the direction of better understanding of Parallel Power Flow scheme, closed loop simulation and analysis of AC/DC converter. Various topologies have been discussed, in terms of advantages, disadvantages, technology and current implementation status. Emphasis of the project has been the design of 200W AC/DC converter with high input power factor and tight output voltage regulation.

II. POWERFACTOR CORRECTION TECHNIQUES

A. Classification of PFC Techniques

The various methods of power factor correction can be classified as:

1. Passive power factor correction techniques
2. Active power factor correction techniques

1. Passive Power Factor Correction Techniques

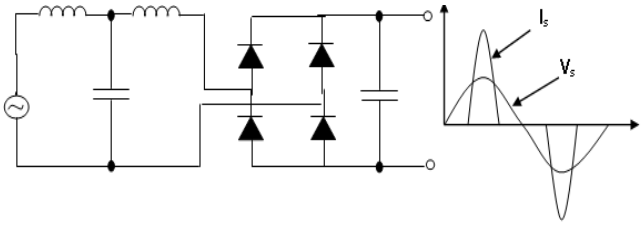

Fig1 the Passive Power Factor Correction

In this approach, an LC filter is inserted between the AC mains line and the input port of the diode rectifier of AC/DC converter as shown in Figure 1. This technique is very simple and rugged but it has bulky size and heavy weight and the power factor cannot be very high. Therefore it is now not applicable for the current trends of harmonic norms. But it is applicable for power rating of lower than 25W. For higher power rating it will be bulky.

2. Active Power Factor Correction Techniques

In this approach, switched mode power supply (SMPS) technique is used to shape the input current in phase with the input voltage. So the power factor can reach up to unity. Figure 2.2 shows the circuit diagram of basic active power correction technique. There are different topologies for implementing active power factor correction techniques. But in this technique, power factor correcting cell is used for tracking the input current in phase of input voltage such that input power factor come up to unity. Comparing with the passive PFC techniques to active PFC techniques has many advantages such as, high power factor, reduced harmonics and smaller size. However, the complexity and relatively higher cost are the main drawbacks of this approach.

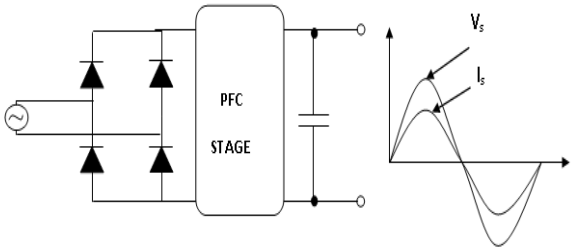

Fig 2 the Active Power Factor Correction

III. SINGLE PHASE ACTIVE POWER FACTOR CORRECTION

Conventional *ON*-line power converters with diode-capacitor rectifier front-end have distorted input current waveform with high harmonic content. They cannot meet the European line-current harmonic regulations defined in the IEC 1000-3-2 document nor the corresponding Japanese input-harmonic current specifications. To meet the above norms, it is to add a power factor

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corrector of the isolated dc/dc converter section of the switching power supply. so again another dc/dc converter is needed for output voltage regulation. So these two converters are needed for single-phase active power factor correction for the requirement of high input power factor and tight output regulation.

There are two techniques for single-phase active power factor correction:

1. two-stage scheme
2. single-stage scheme

A. Two-Stage Approach of Active Power Factor Correction

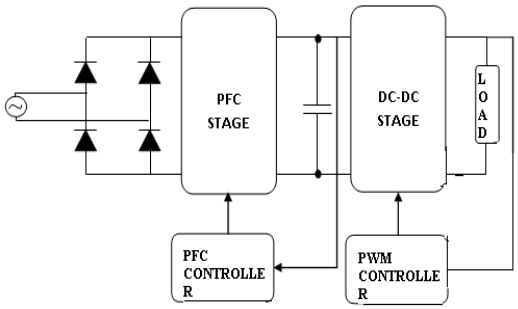

Fig. 3 Block diagram of two stage PFC converter

Two-stage approach is commonly used approach in high power applications. the block diagram of two stage pfc converter is shown in figure.3.1. in this approach, there are two independent power stages. the front-end of pfc stage is usually a boost or buck- boost (or flyback) converter. The dc/dc output stage is the isolated output stage that is implemented with one switch, which is controlled by an independent pwm controller to tightly regulate the output voltage. the two-stage scheme is a cost-effective technique in high power applications; its cost-effectiveness is diminished in low-power applications due to the additional pfc power stage and control circuits.

B. Single- Stage Approach of Active Power Factor Correction

A single-stage scheme combines the PFC circuit and DC/DC power conversion circuit into one stage. A number of single-stage circuits have been reported in recent years. Figure 3.2 shows the block diagram of single-stage approach. Compared to the two-stage scheme, the single-stage approach uses only one switch and controller to shape the input current and to regulate the output voltage. Even though for a single-stage PFC converter, attenuation of input-current harmonics is not as good as for the two-stage approach. But it meets the requirements of IEC 1000-3-2 norms. Again it is cost effective and compact with respect to two stage approach.

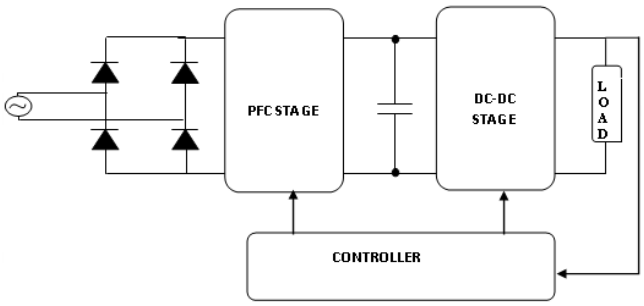

Fig 4 the Block Diagram of Single-Stage PFC Converter

IV. PARALLEL POWER TRANSFER SCHEME

Parallel-connected PFC approach is proposed to overcome the disadvantages of the two schemes in cascade (AC to DC and DC to DC) as well as to meet the design requirement as mentioned. The proposed scheme employs a forward converter and flyback converter. The purpose of forward converter with 60% power rating is to regulate output voltage and flyback converter with 40% power rating is able to regulate input current. The flyback converter operates with continuous conduction mode (CCM) in input inductor current. The input diode current of the forward converter has tailed waveform in which reverse recovery loss can be minimized. The goal of the proposed PFC scheme is to reduce the passive component size to improve total efficiency. Simulation results shows that the proposed scheme is capable of offering good power factor correction and fast dynamic response.

V. OPERATION OF THE PROPOSED TOPOLOGY

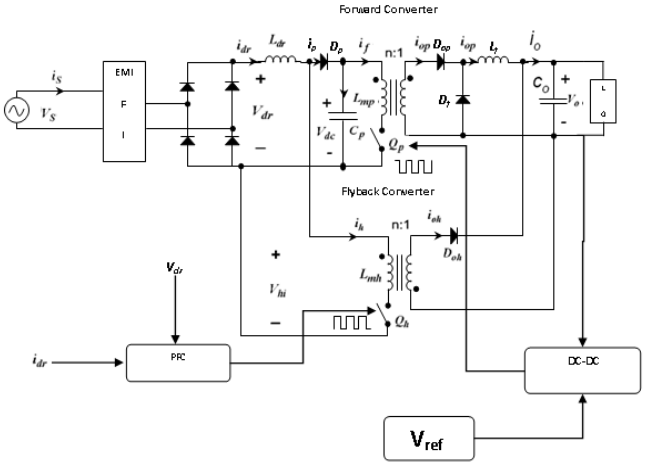

Fig 5 Single-Stage Parallel PFC Converter

Figure.5 shows the proposed parallel-connected PFC scheme which employs a diode rectifier, dc-link capacitor, and a flyback converter in parallel with forward converter. The function of a forward converter with an electrolytic capacitor is to support output voltage regulation. Here the flyback converter fulfills the function of power factor correction by making input current sinusoidal and regulating dc-link voltage.

The two converters operate such that the switching instants are phase-shifted over a switching period i.e. when forward converter switch Q_p is *ON*, the flyback converter switch Q_h remains *OFF* and vice-versa. The flyback converter operates with continuous conduction mode in both an input inductor and a flyback transformer.

The dc-link voltage in this technique can be lower than other approach as

$$V_{dc} = \sqrt{2}\, V_s \qquad (1)$$

The transfer function of flyback converter is expressed as

$$M = \frac{V_o}{V_{dr}} = \frac{D}{D(1-n)} \qquad (2)$$

Where D is the duty ratio of the switch Q_h, n ($=N_p/N_s$), is defined as the ratio of N_p to N_s, and N_p and N_s denote the number of turns of primary and secondary side, respectively.

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$$i_{dr} = i_p + i_h, \quad (3)$$

$$V_{Ldr} = L_{dr}\frac{di_{dr}}{dt}, \quad (4)$$

$$V_{hi} = V_{dr} - V_{Ldr}, \quad (5)$$

$$V_{h1} = V_{hi} - V_{Qh}. \quad (6)$$

Where i_{dr}, i_p and i_h are the rectified, forward converter, and flyback converter input currents on dc side. Since the two input currents i_p and i_h, are interleaved then input current i_{dr} ripple can be simultaneously reduced.

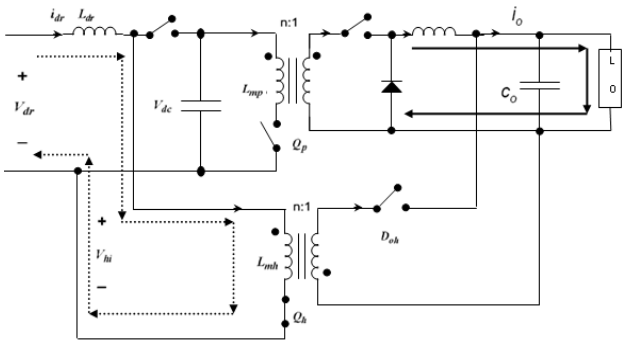

Fig 6 Forward Converter Switch Q_p is *OFF* and Qh is ON

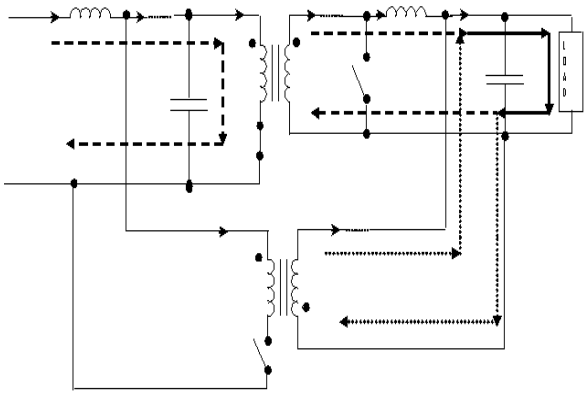

Figure 7 Forward Converter Switch Q_p is *ON* and Qh is OFF

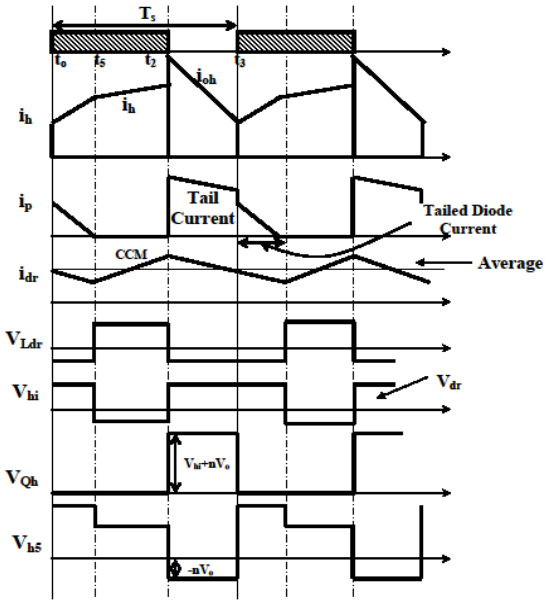

Figure.8 Operational waveforms of the proposed topology

VI. MATLAB SIMULATION RESULTS

A. Parallel PFC Converter Simulation Output

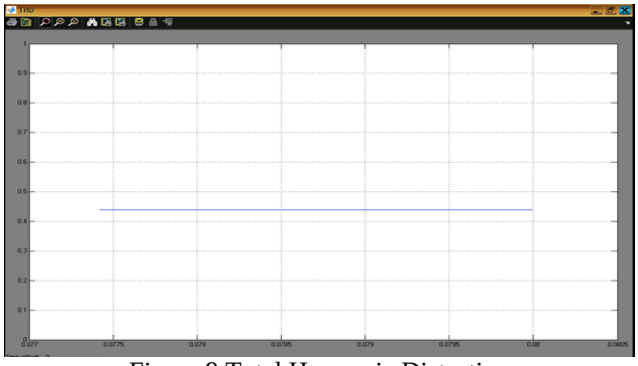

Figure 9 Total Harmonic Distortion

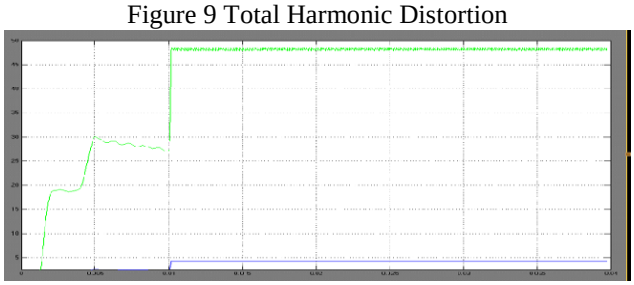

Figure 10 Output voltage & current

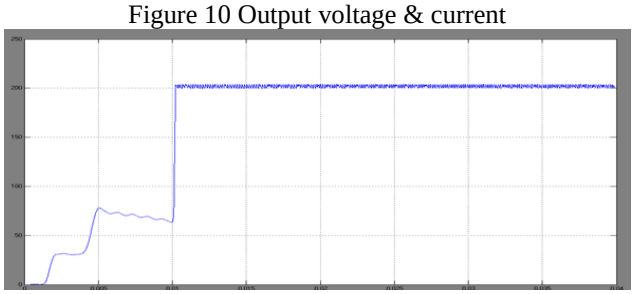

Figure 11 Output power Fly Back Converter Simulation Output

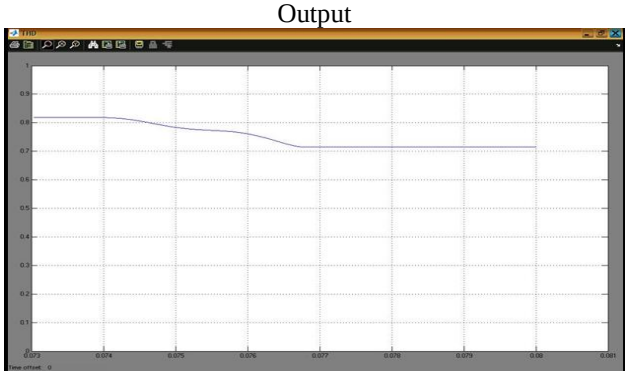

Figure 12 Total Harmonic Distortion

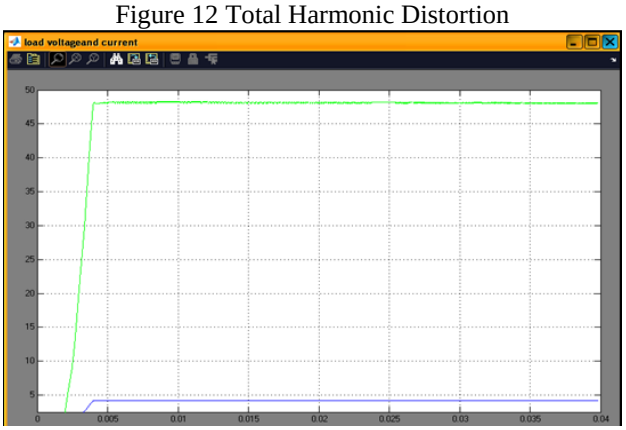

Figure 13 Output voltage and current

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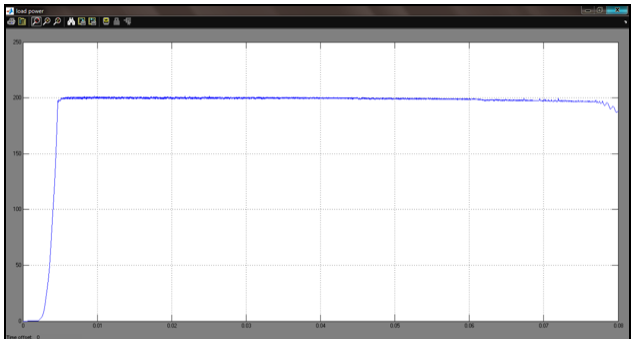

Figure 14 Load power

CONCLUSION

In this paper a parallel –connected single phase power factor correction topology using forward and fly back converter has been proposed. It has been shown that output voltage regulation is achieved by dc-dc stage and input power factor correction is achieved by PFC-stage.

From the discussions in this report, it is clear that the power factor correction is being given considerable importance for low and medium power applications. Also seeing that power electronic equipments are increasingly being used, they pretense a serious problem of lower order harmonics on utility side. Among various schemes available for PFC(power factor control), the single stage scheme is preeminent for low and medium power application because of its cost effectiveness, small component size. But in this scheme, there is a serious limitation of high dc link voltage rise under light load condition. This problem can be addressed by using the concept of Parallel Power Flow.

From the simulation results of Parallel Power Flow topology, it is clear that parallel handing out of power is an effective way to control high dc link voltage and hence reduces the component stresses. This topology also maintains a high input power factor and a tight output voltage regulation without compromising with high DC bus voltage. Furthermore, the efficiency of overall power conversion is high.

Input voltage = 150 V_{P-P}
Load voltage= 48 V
Load current= 4.16A
Power factor= 0.9973
THD= 0.43%

From the above discussions, it is concluded that the Parallel Power Flow Approach is best suited for the power factor correction and results show the performance.

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