Design and Study of Enhanced Parallel FIR Filter using Various Adders for 16 Bit Length

D.Ashok Kumar, P.Samundiswary

Abstract*— Now a day's parallel Finite Impulse Response (FIR) filter plays very important role in the Digital Signal Processing (DSP) based applications. FIR filters are one of the most widely used fundamental filters in the DSP systems. The parallel FIR filters are derived from FIR digital filter. In this paper, design and study of enhanced parallel FIR filter with various adders using the structure of Fast FIR Algorithm (FFA) based FIR filter and symmetric convolution based FIR filter structures considering 2-parallel and 3-parallel filters is done. These entire filter structures are also designed using Ripple Carry Adder (RCA), Carry save Adder (CSA) and Carry Increment Adder (CIA) by replacing the existing adders with the input bit length and coefficient length of 16-bits. Then the performance metrics of the above two structures is done by designing using Verilog HDL. Further, they are simulated and synthesized using Xilinx ISE 13.2 for Vertex family device of speed -12.

Index Terms*— Parallel FIR filter, FFA, symmetric convolution, Ripple Carry Adder (RCA), Carry Save Adder (CSA), Carry Increment Adder (CIA).

I. INTRODUCTION

Fir filters are one of two primary types of digital filter. One is the FIR and another one is IIR filter. Due to the explosive growth of multimedia applications, the demand for high performance and low-power DSP system is increasing day by day. Finite Impulse Response (FIR) digital filters are one of the most widely used fundamental block in DSP applications. Some applications such as error correction and detection, video processing and data compression require the FIR filter to be operated at high frequencies, where as some other applications namely Multiple-input Multiple-output (MIMO) system used in wireless communication require a low-power circuit. The MIMO system requires high throughput FIR filter. Parallel filter structure is a well-known technique for FIR digital filter in terms of area performance analysis.

Recently, a lot of research has been done on the study and analysis of parallel FIR filter based FFA and symmetric convolution structures to achieve better performance. Many researchers are focussing on the design of different structures of parallel FIR filter to meet the needs of current Very Large Scale Integration (VLSI) industry. In parallel FIR filter, Single Input to Single Output (SISO) is converted into Multiple Input to Multiple Output (MIMO). In parallel FIR filter, there are two types of structures.

First type is the FFA structure and the second type is the symmetric convolution based FIR filter structure. In FFA, the techniques used are dividing and conquer.

In the symmetric convolution structures, reusability & poly phase decomposition are used that reduces the number of multiplication in sub filter section by exploiting the inheritance nature of symmetric coefficients compared to that of FFA based parallel FIR filter.

S.Balasubramaniam et.al [1, 14] discussed about the design of 2-parallel FIR filter structures. Yu-Chi Tsao et.al [2, 3, 4] discussed about parallel linear FIR filter based on odd and even length. In this paper, design and performance analysis of FFA and symmetric convolution based FIR filter structures considering 2-parallel and 3-parallel filters for bit length and coefficients of 16 bits is done by incorporating various adder topologies.

This paper is organized as follows: Section I deals with introduction & related work. In section II, parallel FIR filter structures using FFA and symmetric convolution techniques are explained. In section III, design of parallel FIR filter with various adders is discussed. And section IV deals with simulation and synthesis results of modified parallel FIR filter structures with adders such as RCA,CSA, CIA for 16 bit length . Conclusion and future work are drawn in section V.

II. PARALLEL FIR FILTER

Parallel FIR filters [5] are designed using the FFA & symmetric convolution structures for 2*2 parallel and 3*3 parallel filters. The 2*2 parallel FIR filter contains two inputs (X_0, X1), coefficients (H0, H1) and outputs (Y_0, Y1). The 3*3 parallel FIR filter contains three filter inputs (X_0,X_1,X_2), three filter coefficients (H_0,H_1,H_2), and three filter outputs (Y_0,Y_1,Y_2).

A.Fast FIR Algorithm (FFA)

In general, n-tap FIR filter in time domain equation is given below (1)

$$Y(n) = \sum_{i=0}^{N-1} h(i)x(n-1),\ n=0,1,2,3\ldots..\infty \qquad (1)$$

Here h(n) and x(n) are finite duration elements.

In two parallel FIR filter, the elements present in the structure are already discussed. Parallel FIR filter is derived from polyphase decomposition [6]

$$\sum_{p=0}^{L-1} Y_P(z^L)z^{-P} = \sum_{q=0}^{L-1}\left(z^L z^{-q}\sum_{r=0}^{L-1} H_r(z)z^{-r}\right) \qquad (2)$$

where

$X_q=\sum_{q=0}^{\infty} z^{-k}X(L_{k+q})$,

$H_r=\sum_{k=0}^{(N/l)} z^{-k}X(L_{k+r})$,

$Y_p=\sum_{k=0}^{\infty} z^{-k}X(L_{k+p})$.

Manuscript Received on May 2014.

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B. 2*2 FFA Based Parallel FIR filter structure (L=2)

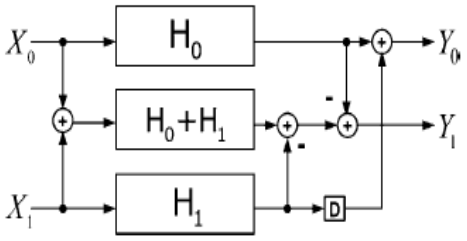

Fig.1.Two parallel FIR filter structure

The two parallel FIR filter structure is shown in Fig.1.The output equation for this filter structure [7] is

$Y_0= H_0 X_0 - Z^{-2}H_1X_1$ (3)

$Y_1= (H_0+H_1) (X_0+X_1)-H_0X_0-H_1X_1$ (4)

This structure contains the two outputs and the outputs are obtained using three length N/2 FIR filter and four pre/post processing adders. Further the outputs (Y_0 and Y_1) are determined through the terms of X_0H_0 and $X1H_1$.

C. 3*3 FFA based parallel FIR filter structure (L=3)

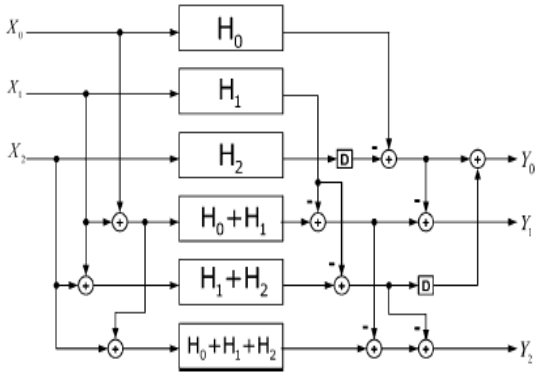

Fig.2.Three parallel FFA filter structure

The three parallel FIR filter structure is shown in Fig.2.The output equation for this filter structure is

$Y_0= H_0 X_0 - Z^{-3}H_2X_2+Z^{-3} * [(H_1+H_2) (X_1+X_2) - H_1X_1]$ (5)

$Y_1= [(H_0+H_1) (X_0+X_1) –H_1X_1] - (H_0X_0-Z^{-3}H_2X_2)$ (6)

$Y_2= [(H_0+H_1+H_2) (X_0+X_1+X_2)] - [(H_0+H_1) (X_0+X_1) -H_1X_1] [(H_1+H_2) (X_1+X) - H_1X_1]$. (7)

These structures contain the three outputs and 3N multiply units and (3N-1) adders similarly to the simple two parallel FIR filters having the pre/post adders. In the three parallel FIR filter structure, the outputsY_0, Y_1 and Y_2 are obtained through the input and coefficients in terms of $X_0 H_0$, $X_1 H1$, and $X_2 H2$. These three terms need to be computed only once which means they required six number of filtering operations.

D. 2*2 Symmetric convolution based parallel FIR filter structure (L=2)

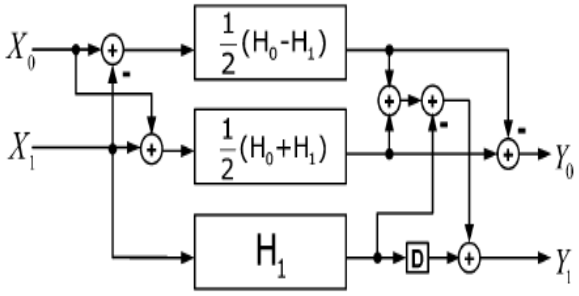

Fig.3.Two parallel symmetric convolution filter structure

The two parallel symmetric convolution based FIR filter structure is shown in Fig.3.Output equation for this filter structure [8,9] is given below,

$Y_0= \{1/2[(H_0+H_1) (X_0+X_1)+(H_0-H_1)(X_0-X_1)]-H_1X_1\}+ Z^{-2}H_1X_1$ (8)

$Y_1=1/2[(H_0+H_1) (X_0+X_1)-(H_0-H_1) (X_0-X_1)]$ (9)

E. 3*3 Symmetric convolution based parallel FIR filter structure (L=3)

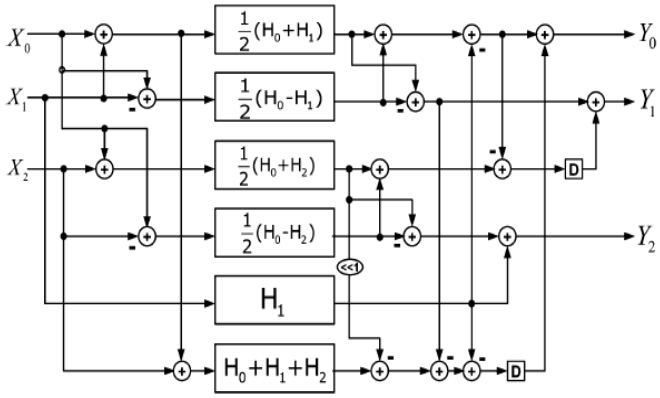

Fig.4.Three parallel symmetric FIR filter structure

The three parallel symmetric convolution based FIR filter structure is shown in Fig.4.Output equation for this FIR filter structure is given in eq. 10, 11& 12.

$Y_0=1/2[(H_0+H_1)(X_0+X_1)+(H_0-H_1)(X_0-X_1)]H_1X_1+Z^3\{(H_0+H_1+H_2)(X_0+X_1+X_2)-(H_0+H_2)(X_0+X_2)-(H_0-H_1)(X_0+X_2)-1/2[(H_0+H_1](X_0+X_1)-(H_0-H_1)(X_0-X_1)]-H_1X_1\}$ (10)

$Y1=1/2[(H_0+H_1)(X_0+X_1)-(H_0-H_1)(X_0-X_1)]+Z^3\{1/2[H_0+H_2)(X_0+X_2)+(H_0-H_2)(X_0-X_2)]-1/2[(H_0+H_1)((X_0+X_1)+(H_0-H_1)(X_0-X_1)]+H_1X_1\}$ (11)

$Y2=1/2[(H_0+H_2) (X_0+X_2)-(H_0-H_2)(X_0-X_2)]+H_1X_1$ (12)

III. PARALLEL FIR FILTER WITH VARIOUS ADDERS

Adders are categorized depending upon the carry occurred in the addition of two n bit numbers.

A. Ripple Carry Adder

A n-bit ripple carry adder consists of n full adders with the carry signal propagating from one full adder stage to next stage from LSB bit to MSB bit.

The critical path of the ripple carry adder consists of the carry chain from the first Full adder stage to the last. A 8-bit ripple carry adder structures is shown in Fig.5

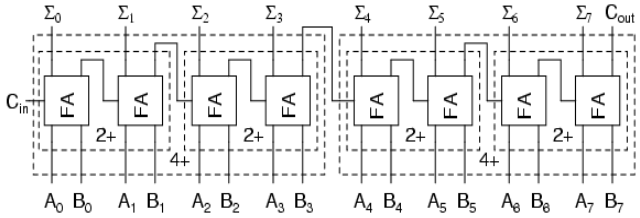

Fig.5.RippleCarryAdder

B. Carry Save Adder

A carry-save adder illustrated in fig. 6 is a type of digital adder. Compute the sum of three or more *n*-bit numbers of binary bits. It differs from other digital adders in that it outputs two numbers of the same dimensions as the inputs, one which is a sequence of partial sum bits and another one is a sequence of carry bits.

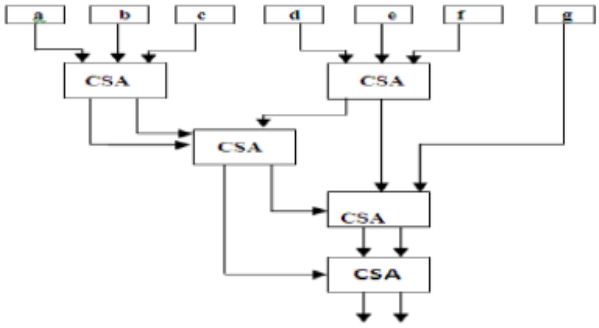

Fig. 6. Carry save adder

C. Carry Increment Adder

The design of Carry Increment Adder (CIA) consists of RCA's and incremental circuitry .The incremental circuit can be designed using half adder's in ripple carry chain with a sequential order. The addition operation is done by dividing total number of bits in to group of 4bits and addition operation is done using several 4bit RCA's. The architecture of CIA is shown in Fig.7.

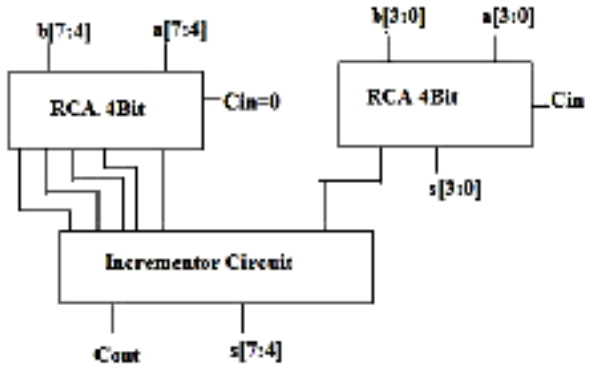

Fig.7.Carry Increment adder

IV. SIMULATION RESULTS

Parallel FIR filters using FFA and symmetric convolution structures are designed by using Verilog HDL. Then, simulation and synthesis [10] of the above mentioned structures are done by using Xilinx ISE 13.2 for virtex4 family device with a speed grade of -12. In simulation results, Technology View [11] describes top block which shows the set of inputs and outputs. Register Transfer Logic (RTL) view designates the internal architectural blocks along with the connections between input and output pins. Timing waveform [12, 13] is generated by writing test bench program which contains the set of input test vectors applied to design.

A. Simulation results of two-parallel 16-bits FFA based FIR Filter using RCA

RTL view and technology view is shown in the Fig 8 and Fig.9. The timing waveform of two parallel FFA based FIR filter with RCA shown in Fig.10 represents the output obtained from various input vector provided in the test bench program during simulation process. Output also depends on the clock and reset values.

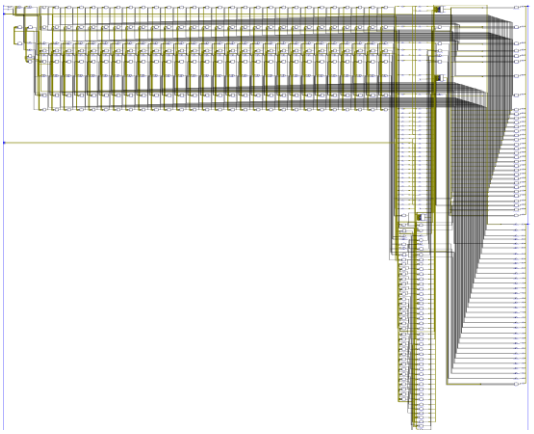

Fig. 8.RTL view of two parallel 16 bits FFA based FIR filter using RCA

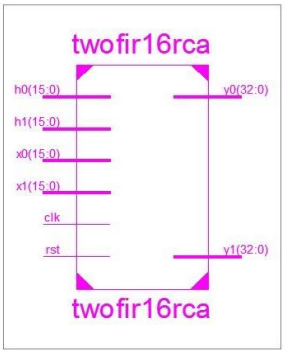

Fig.9.Technology view of two parallel 16 bits FFA based FIR filter using RCA

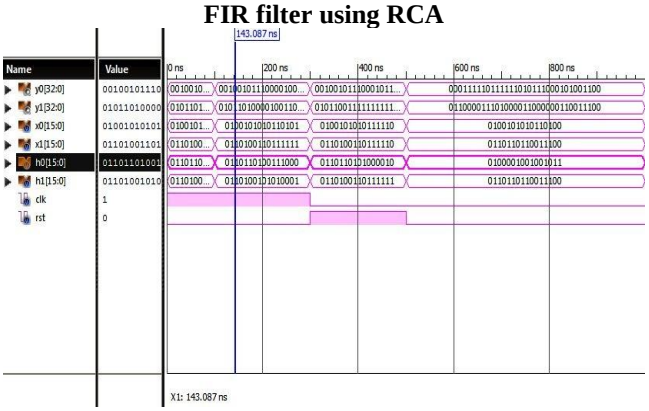

Fig.10.Timing wave form of two parallel 16 bits FFA based FIR filter using RCA

B. Simulation results of two-parallel 16-bits FFA based FIR Filter using CSA

RTL view and technology view is shown in Fig.11 and Fig.12. The timing waveform of two parallel FFA with CSA shown in Fig.13 represents the output obtained from various input vectors provided in the test bench program during simulation process. Output also depends on the clock and reset values.

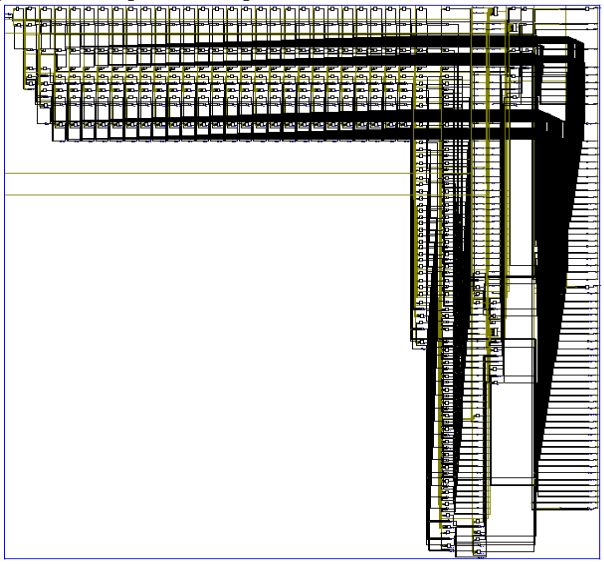

Fig.11.RTL view of two parallel 16 bits FFA based FIR filter using CSA

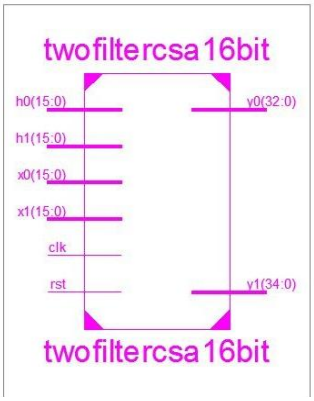

Fig.12.Technology view of two parallel 16 bits FFA based FIR Filter using CSA

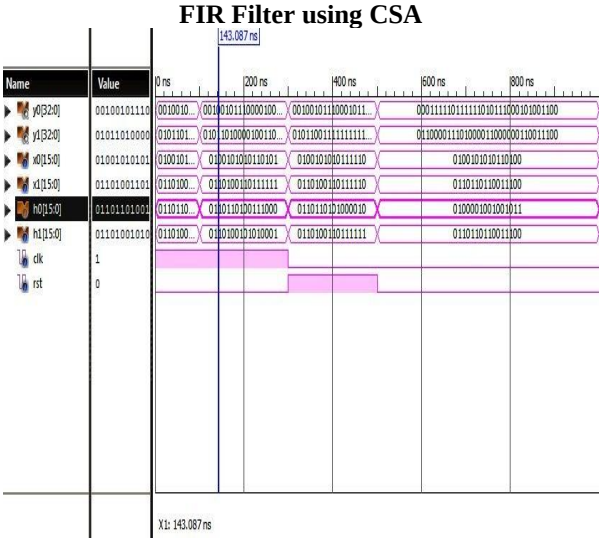

Fig.13. Timing wave form of two parallel 16 bits FFA based FIR filter using CSA

C. Simulation results of two-parallel 16-bits FFA based FIR Filter using CIA

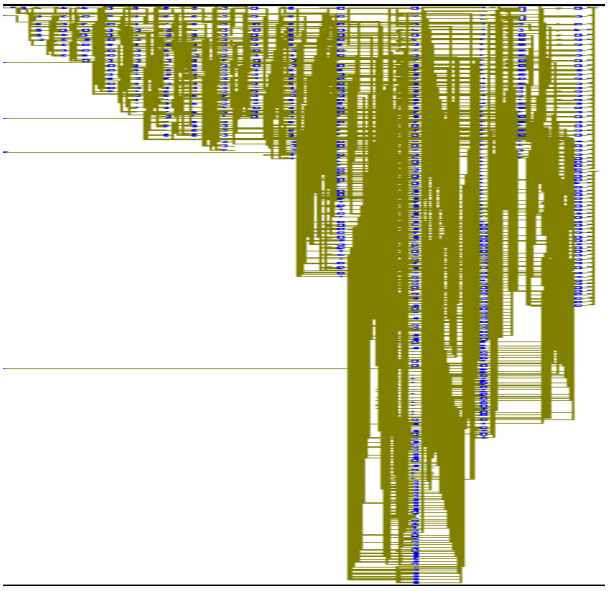

Fig.14.RTL view of two parallel 16 bits FFA based FIR filter using CIA

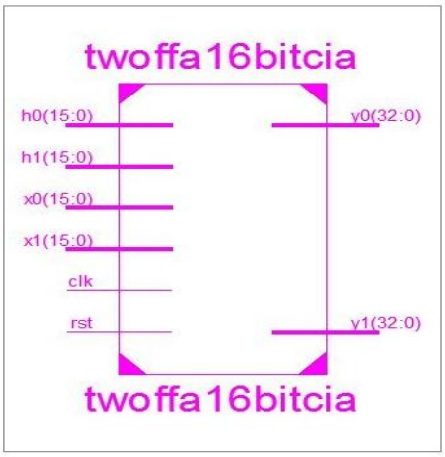

Fig.15.Technology view of two parallel 16 bits FFA based FIR filter using CIA

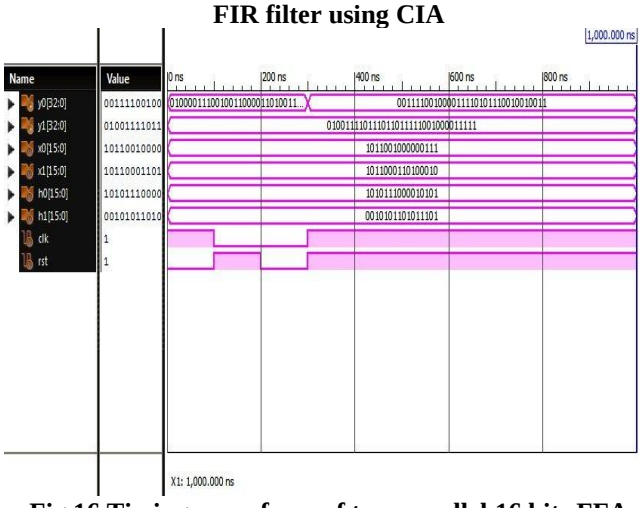

Fig.16.Timing wave form of two parallel 16 bits FFA based FIR filter using CIA

RTL view and technology view is shown in Fig.14 and Fig.15. The timing waveform of two parallel FFA with CIA shown in Fig.16 represents the output obtained from various input vectors provided in the test bench program during simulation process. Output also depends on the clock and reset values.

D. Simulation results of three-parallel 16-bits symmetric convolution FIR Filter using CSA

Technology view is shown in the Fig.17. And RTL view is shown in Fig.18.The timing waveform of three parallel symmetric convolution based FIR filter with CSA shown in Fig.19 represents the output obtained from various inputs vector provided in the test bench program during simulation process. Output also depends on the clock and reset values.

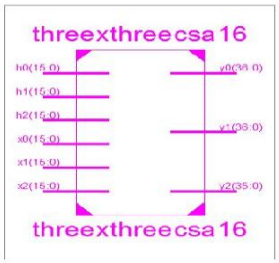

Fig.17.Technology view of three parallel 16 bits symmetric convolution based FIR filter using CSA

Fig.18. RTL view of three parallel 16 bits symmetric convolution based FIR filter using CSA

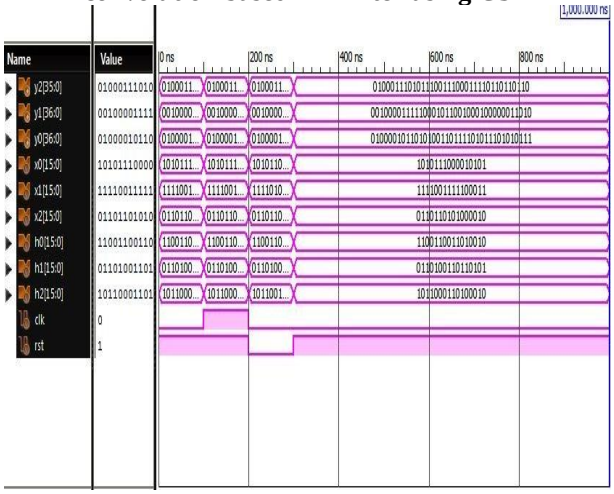

Fig.19.Timing wave form of three parallel 16 bits symmetricconvolution based FIR filter using CSA

E. Simulation results of three-parallel 16-bits symmetric convolution FIR Filter using CIA

RTL view is shown in the Fig.20. And technological view is shown in Fig.21.The timing waveform of three parallel symmetric convolution based FIR filter with CIA shown in Fig.22 represents the output obtained from various input vector provided in the test bench program during simulation process. Output also depends on the clock and reset values.

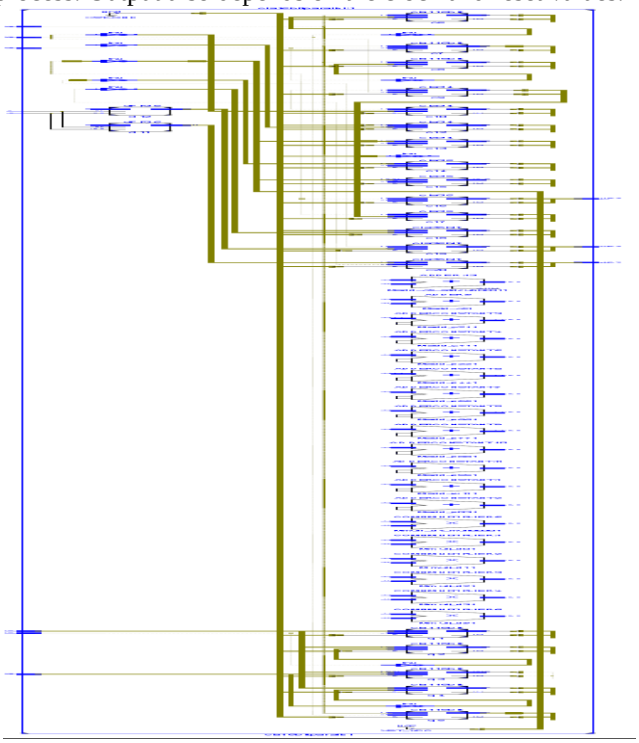

Fig.20.RTL view of three parallel 16 bits symmetric convolution based FIR filter using CIA

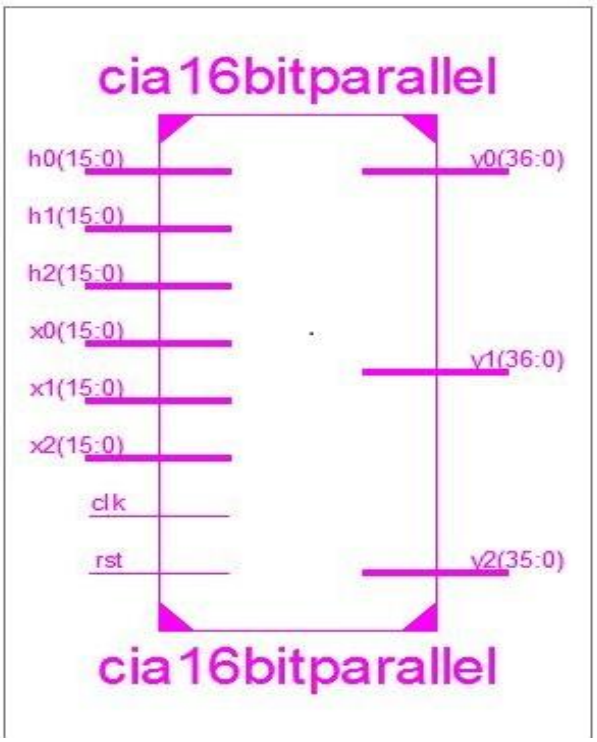

Fig.21.Technology view of three parallel 16 bits symmetric convolution based FIR filter using CIA

Fig.22.Timing wave form of three parallel 16 bits symmetric convolution based FIR filter using CIA

***F.* Simulation results of three-parallel 16-bits symmetric convolution based FIR Filter using RCA**

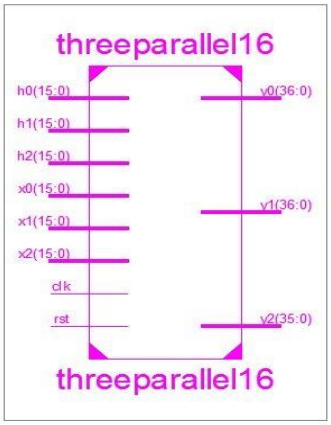

Fig.21.Technology view of three parallel 16 bits symmetric convolution based FIR filter using RCA

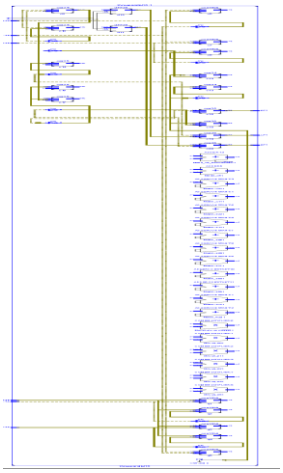

Fig.24.Technology view of three parallel 16 bits symmetric convolution based FIR filter using RCA

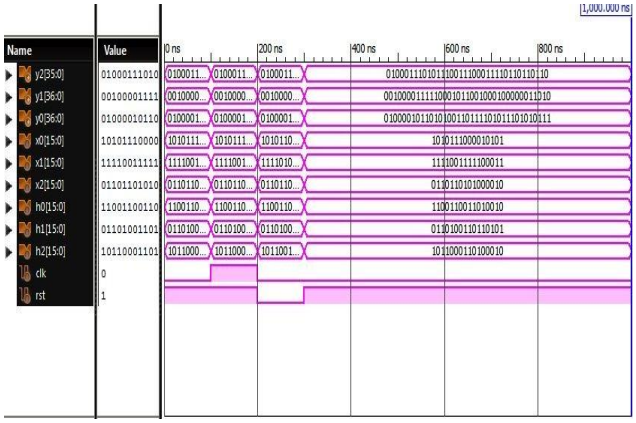

Fig.25.Timing wave form of three parallel 16 bits symmetric convolution based FIR filter using RCA

***G.* Performance analysis of FFA and Symmetric convolution structured based FIR filter for16-bit length with various adders**

The performance comparison of FFA and Symmetric convolution structured based FIR filter for16-bit length with various adders such as RCA, CSA and CIA are discussed in the form of Tabular column.

TABEL I. PERFORMANCE COMPARISON OF FFA BASED FIR FILTERWITH VARIOUS ADDERS (16 BITS)

Structure	Type of adder	delay(ns)		Area(slices)	
		L=2	L=3	L=2	L=3
Symmetric convolution	RCA	42.123	30.623	240	132
	CSA	37.03	28.75	270	142
	CIA	27.144	27.542	289	583

From the above table I, it is observed that FFA structure based FIR filter for 16-bit input data and coefficients using RCA has better area compared to that of CSA & CIA. And, CIA has better in terms of delay compared to that of RCA & CSA.

TABEL II. PERFORMANCE COMPARISON OF SYMMETRIC CONVOLUTION BASED FIR FILTER WITH VARIOUS ADDERS (16 BITS)

Structure	Type of adder	delay(ns)		Area(slices)	
		L=2	L=3	L=2	L=3
Fast FIR Algorithm	RCA	20.629	40.212	22	148
	CSA	14.642	29.719	32	165
	CIA	12.448	26.214	45	516

From the above table II, it is observed that symmetric convolution based FIR filter for 16-bit input data and coefficients using RCA has better area compared to that of CSA & CIA. And, CIA has better in terms of delay compared to that of RCA & CSA

V. CONCLUSION AND FUTURE WORK

In this paper, FFA based FIR filter structure and symmetric convolution structure based FIR using RCA, CSA and CIA with the input bit length of 16-bits is designed using Verilog HDL. These structures are simulated in Xilinx 13.2 using the family virtex4 speed -12 device. It is concluded through the simulation results, that symmetric convolutions and FFA based FIR filter structure using CIA is better compared to that of RCA & CSA in terms of delay analysis. In area analysis, RCA shows better results compared to that of CSA & CIA, in the above mentioned structures. In future, the work can be extended from 3 parallel structures to 6 parallel structures by using cascading algorithm.

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