Design and Analysis of Semi-Empirical Model Parameters for Short-Channel CMOS Devices

Magnanil Goswami, Sudakshina Kundu

Abstract*: Recently analog circuit designers are interested in structured optimization techniques to automate the process of CMOS circuit design. Geometric programming, which makes use of monomial and posynomial expressions to model MOSFET parameters, represents one such approach. The extent of accuracy in finding a global optimal solution using this approach depends on the formulation of circuit and device equations as monomials and posynomials. Being pivotal in determining device transfer characteristic, transconductance and output conductance cast a direct impact on the overall CMOS circuit behavior. In this paper we developed and substantiated high fidelity expressions of transconductance and output conductance for short-channel MOSFETs in monomial form.

Index Terms*: Analog CMOS circuit, geometric programming, global optimal solution, short-channel MOSFET, structured optimization.

I. INTRODUCTION

With the advancements in submicron CMOS process technology; analog circuits play an important role in the production of SOCs (system on chip) [1]. Constant downscaling of the device dimensions invokes several detrimental factors such as larger parasitics and short-channel effects; turning analog CMOS circuit design into a very cumbersome affair [1], [2]. Depending on how circuit performance and constraints are evaluated, automatic analog circuit synthesis as an aid to improve the designer's productivity is broadly classified into simulation-based and equation-based optimization [3], [4]. Our discussion converges on the equation-based optimization technique, where the analog circuit design problem is dismantled and formulated as a set of objective and constraint functions to be optimized conjointly [1]. Such structured optimization techniques can produce prompt optimal solutions [1], [3]. Geometric programming [3], [4], [5] is one such semi-empirical structured optimization technique which is extensively used in finding globally optimal solutions to CMOS analog circuit design problems. Though, the accuracy of this global optimality relies on the exactness in formulating the objective and constraint functions [3], [5]. It is observed from prior literatures [4], [6], [7] that the optimization of CMOS analog circuits requires several approximations at the transistor-level, when formulated using geometric programming. In this paper, we considered MOSFET transconductance and output conductance, two important small-signal parameters; and augmented high fidelity monomial expressions from the respective analytical expressions; considering some of the major short-channel effects such as velocity saturation and channel-length modulation. Our selective case study aims to incorporate more accurate MOSFET performance equations pertaining to the CMOS circuit optimization problem; comprising of objective and constraints for geometric programming. This paper is organized as follows. In section II, we briefly elaborate the method of geometric programming. Expressions for transconductance and output conductance of the short-channel MOSFET are deduced from the analytical solutions in section III. Owing to the analytical solutions, monomial models of device transconductance and output conductance are formulated in section IV. In section V, these monomial models are evaluated using fitting data obtained from SPICE level 3 CMOS processes for 90 nm and 180 nm technology nodes and tallied with respective values calculated from the analytical solutions for relative error estimation. Finally, our discussion is inferred in section VI.

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II. GEOMETRIC PROGRAMMING

Geometric programming is a special form of objective and constraint function based convex optimization problem [3], [5]. The fundamental idea of modeling any practical problem using this method is to express the design objective and constraints in a commensurate manner prior to taking them for optimization. The modeling may take place in two ways; either by exact formulation or by approximation. Although it is not certain whether every design aspect can be formulated as a compatible function, but any practical problem, when duly formulated, can be solved globally using the highly efficient primal dual interior-point method [5]. The objective and constraints are either represented by a monomial and/or a posynomial (i.e., a positive polynomial) and/or a positive fractional power or pointwise maximum of posynomials [3], [5]. Geometric optimization problem is of the form:

$$\begin{aligned} &\text{optimize} && f_0(x) \\ &\text{subject to} && f_i(x) \le 1, && i = (1,\ldots,m) \\ &&& g_i(x) = 1, && i = (1,\ldots,p) \\ &&& x_i > 0, && i = (1,\ldots,n) \end{aligned} \qquad (1)$$

where $f_1,\ldots,f_m$ are posynomial constraints and $g_1,\ldots,g_p$ are monomial constraints of the vector x comprising n real positive variables $x_1,\ldots,x_n$.

The objective function f_0 is either a posynomial to minimize (only) or a monomial to maximize or minimize (scenario specific). A function $g(x)$: $\mathbf{R}^n \rightarrow \mathbf{R}$ is said to be a monomial [3], [5] if its domain is the set of vectors with positive components and its values take a form given by the following power law expression:

$$g(x) = cx_1^{a_1} \ldots x_n^{a_n} \tag{2}$$

where $c > 0$ is the coefficient and the vector $a = a_1,\ldots,a_n$ is the exponent of the monomial. A function $f(x)$: $\mathbf{R}^n \rightarrow \mathbf{R}$ is said to be a posynomial [3], [5] if its domain is the set of vectors with positive components and its values take a form of non-negative sum of monomials:

$$f(x) = \sum_{k=1}^{K} c_k g_k(x) \tag{3}$$

where $g_k(x)$ are monomials and $c_k \geq 0$ for $k = 1,\ldots K$.

III. ANALYTICAL EXPRESSIONS

Analog CMOS circuit performance measurements fall in two categories: small signal (linear) and large signal (non-linear) analyses [8]. The process of apprehending the circuit for geometric programming involves expressing some or all of the small and large signal parameters as monomials and/or posynomials. Our discussion encompasses on a subset of MOSFET small signal parameters comprising transconductance (g_m) and output conductance (g_d) to fuel arguments regarding monomial models based on short-channel MOSFET data. The piecewise-continuous equations of drain current for triode and saturation regions [2] considering body effect, velocity saturation, channel length modulation, are given by the following equation duo:

$$I_{Dtriode} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) \frac{V_{od} V_{ds} - \frac{m}{2} V_{ds}^2}{1 + \left(\mu_{eff} V_{ds}\right) / \left(2 v_{sat} L\right)} \tag{4}$$

$$I_{Dsat} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) \frac{V_{od}^2 / (2m)}{1 + \mu_{eff} V_{od} / (2m v_{sat} L)} \left(1 + \lambda V_{ds}\right) \tag{5}$$

where C_{ox} is the gate oxide capacitance per unit area, W is the channel width, L is the channel length, V_{ds} is the drain-to-source voltage, v_{sat} is the carrier saturation velocity, λ is the channel-length modulation factor, and V_{od} is the overdrive voltage given by:

$$V_{od} = V_{gs} - V_{th} \tag{6}$$

where V_{gs} is the gate-to-source voltage, and V_{th} is the threshold voltage. The parameter μ_{eff} in (4) and (5) is the effective mobility given by the following equation:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta V_{od}} \tag{7}$$

where μ_0 is the low field mobility, and θ is the mobility degradation factor given by:

$$\theta = \frac{\beta_\theta}{t_{ox}} \tag{8}$$

where t_{ox} is the gate oxide thickness, and β_θ is a fitting parameter; typically ranges between 5E-10 to 20E-10 V^{-1}. The body effect factor m is given as follows:

$$m = 1 + \frac{\sqrt{\frac{\varepsilon_{si} q N_{ch}}{4\psi_B}}}{C_{ox}} \tag{9}$$

where ε_{si} is the permittivity of the silicon substrate, q is the electron charge, N_{ch} is the channel doping concentration, C_{ox} is the oxide capacitance per unit area, and ψ_B is the difference between Fermi potential and intrinsic potential, given by:

$$\psi_B = U_T \ln\left(\frac{N_{ch}}{n_i}\right) \tag{10}$$

where U_T is the thermal voltage; typically 0.0259 V at room temperature, and n_i is the intrinsic carrier concentration; typically 1.5E10 cm^{-3} for silicon at room temperature.

A. Transconductance (g_m)

Transconductance of a MOSFET can be estimated from the following expression:

$$g_m = \left.\frac{\partial I_{Dsat}}{\partial V_{gs}}\right|_{V_{ds}} \tag{11}$$

Using the saturation drain current equation in (5), the expression of transconductance for a short-channel device in saturation can be augmented from (11).

$$g_m = \mu_0 C_{ox} W v_{sat} \left(1 + \lambda V_{ds}\right) \frac{\left(4 m v_{sat} L V_{od} + \left(2 m v_{sat} L\theta + \mu_0\right) V_{od}^2\right)}{\left(2 m v_{sat} L + \left(2 m v_{sat} L\theta + \mu_0\right) V_{od}^2\right)} \tag{12}$$

B. Output Conductance (g_d)

Output conductance of a MOSFET can be estimated from the following expression:

$$g_d = \left.\frac{\partial I_{Dtriode}}{\partial V_{ds}}\right|_{V_{gs}} \tag{13}$$

Using the drain current equation in (4), the expression of output conductance for a short-channel device can be augmented from (13).

$$g_d = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) V_{od} \tag{14}$$

The parameters for estimating g_m and g_d from (12) & (14) are enlisted in Table I. These parameters are adopted from LTspice level-8 Predictive Technology Model (PTM) cards for 90 nm and 180 nm CMOS processes at 300 Kelvin. The mobility degradation factor θ and the channel length modulation factor λ are obtained from the respective current-voltage characteristics of the MOS models.

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TABLE I. PROCESS, GEOMETRY AND BIAS PARAMETERS FOR CALCULATION OF TRANSCONDUCTANCE & OUTPUT CONDUCTANCE

Parameter		90 nm	180 nm
Electron mobility (m^2/V)		1.79E-2	2.88E-2
Saturation velocity (m/s)		1.10E5	9.18E5
Gate-oxide thickness (nm)		2.5	4.1
Channel doping concentration (cm^{-3})		9.70E17	2.35E17
Mobility degradation factor (V^{-1})		0.3	0.2
Channel length modulation factor (V^{-1})		0.4	0.3
Channel length (µm)	min:	0.09	0.18
	max:	0.45	0.9
Channel width (µm)	min:	1	1
	max:	100	100
Gate overdrive voltage (V)	min:	0.1	0.1
	max:	0.4	0.5
Drain to source voltage (V)	min:	0.5	0.6
	max:	1	1.2

TABLE II. FITTING PARAMETERS FOR MONOMIAL EXPRESSIONS

Expression	Fitting Parameter	90 nm	180 nm
g_m	C0	0.0423	0.0463
	C1	-0.4578	-0.4489
	C2	0.5275	0.5311
	C3	0.4725	0.4689
g_d	C4	0.0091	0.0096
	C5	-0.5637	-0.5595
	C6	0.5305	0.5194
	C7	0.4695	0.4806

IV. MONOMIAL BASED SEMI-EMPIRICAL MODELS

Monomial based expressions for transconductance g_m and output conductance g_d are formulated as follows:

$$g_m = C_0 L^{C_1} W^{C_2} I_{ds}^{C_3} \quad (15)$$

$$g_d = C_4 L^{C_5} W^{C_6} I_{ds}^{C_7} \quad (16)$$

where I_{ds} represents the drain to source current and C_0 — C_7 are fitting constants. Equations (15) & (16) are nonlinear in nature and are not likely to be implemented by routine functions of numerical software such as MATLAB. Therefore a logarithmic transformation is performed to convert (15) & (16) into adoptable forms:

$$g_m^* = C_0^* + C_1 L^* + C_2 W^* + C_3 I_{ds}^* \quad (17)$$

$$g_d^* = C_4^* + C_5 L^* + C_6 W^* + C_7 I_{ds}^* \quad (18)$$

where the set of new variables ($g_m^*, g_d^*, L^*, W^*, I_{ds}^*$) and the constants C_0^* & C_4^* represent '*logarithm*' of their respective non-asterisked values in (15) & (16). Thus multiple linear regression analysis, a standard function in MATLAB, can be introduced on (17) & (18) to implement the curve fitting process. Fitting data obtained from above are listed in Table II for both 90 nm and 180 nm technology nodes.

V. RESULT ANALYSIS

It is important to examine the precision of our models by collating the evaluated values of g_m and g_d with that of the analytical solutions for both 90 nm and 180 nm instances; as illustrated in Fig. 1, Fig. 2, Fig. 3, and Fig. 4.

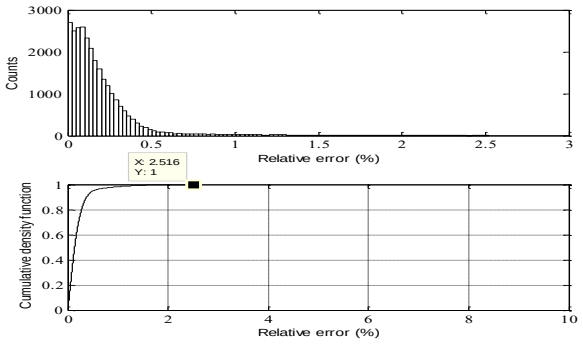

Fig. 1 Histogram and Cumulative Density Function of Relative Error of Curve Fitting: for g_m of 90 nm NMOS

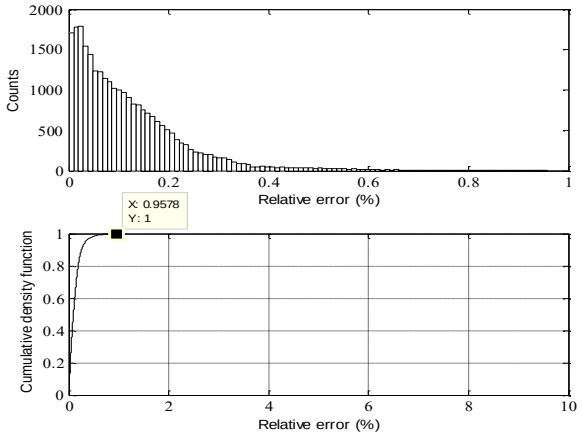

Fig. 2 Histogram and Cumulative Density Function of Relative Error of Curve Fitting: for g_d of 90 nm NMOS

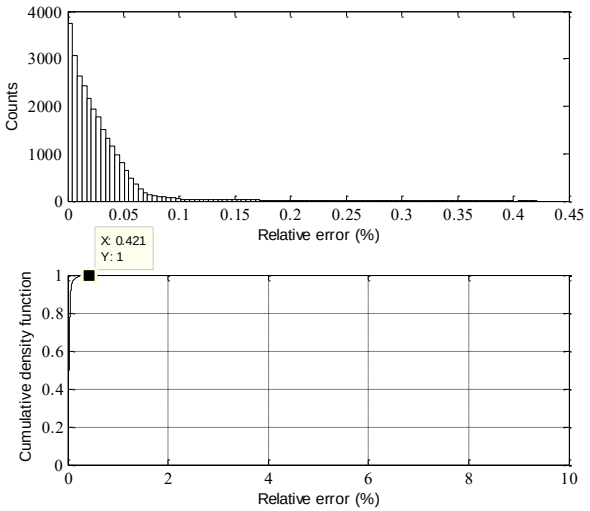

Fig. 3 Histogram and Cumulative Density Function of Relative Error of Curve Fitting: for gm of 180 nm NMOS

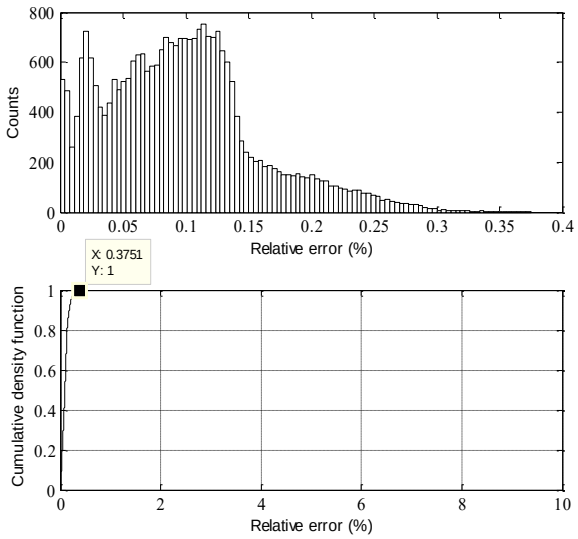

Fig. 4 Histogram and Cumulative Density Function of Relative Error of Curve Fitting: for gd of 180 nm NMOS

TABLE III. SUMMARY OF DESIGN COLLATION

Measurement	g_m		g_d	
	90 nm	180 nm	90 nm	180 nm
Coefficient of determination	0.999	1.0	1.0	1.0
Maximum relative error	2.516%	0.421%	0.9578%	0.3751%

As observed from Table III, coefficient of determination of the transconductance g_m and the output-conductance g_d for both 90 nm and 180 nm CMOS technology nodes are either 1.0 or very close to that. It implies that the overall fitting of our monomial models to the respective analytical solution data is extremely good. Also the maximum relative error in fitting remains very much within admissible proximity for all the four instances.

VI. CONCLUSION & FUTURE SCOPE

Therefore the semi-empirical monomial models proposed herein; can be effectively used for CMOS device and circuit co-optimization using geometric programming. Thus higher fidelity globally optimal solutions can be pertained for analog ICs with little human oversight. Throughout this work, we have practiced that how well our evolved models react to the fetched data. However, generalization may require minimal alteration in terms of fitting parameters to reflect the changes in analytical expressions, if any. Perhaps the probable sources of limitations of this approach are the types of constraints it can handle and the level of dependence of this method on SPICE data. Hence, there is always a room for improvisation through higher precision modeling strategies. Since our monomial models incorporate some of the major short-channel effects with a greater degree of accuracy; they are preferred over the existing alternatives in submicron CMOS device optimization. It is customary to mention that associating the detrimental attributes occurring in deep submicron CMOS process technology nodes to our semi-empirical models can be considered as one of the successive objectives and an inevitable continuation of this investigation.

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