Design of Baugh Wooley Multiplier using HPM Reduction Tree Technique

Jipsa Antony, Jyotirmoy Pathak

Abstract*— Baugh Wooley Multiplier is one of the different techniques for signed multiplication. It is not widely used. Here design and implementation of 8 bit Baugh Wooley multiplier using conventional method as well as using High Performance Multiplier Reduction tree (HPM) technique and the comparative analysis of both the design for power, delay and the area foot print has done using Cadence RTL complier 180nm process technology.

***Index Terms*— Multiplier, Baugh Wooley, HPM, Cadence RTL**

I. INTRODUCTION

Multiplication is one of the complex arithmetic operation [6]. In most of the signal processing algorithms multiplication is a root operation whereas multipliers have large area, consume considerable power and long latency. So, in low-power VLSI system design, low-power multiplier design is also an important part. Mostly architecture of parallel multipliers can be classified into three parts: *bit generation of primary partial product* by using simple AND gates or by using any recoding strategies; *bit compression of partial product* by using any irregular array of logarithmic tree or by using a regular array; and the *final addition* [6]. The main part of this paper is the reduction tree technique which is used for designing a new Baugh Wooley multiplier architecture. High Performance Multiplier (HPM) reduction tree [6] is based mainly on the generated partial product compression [1]. It is completely regular and the connectivity of the adding cells in HPM is in the triangular shape. The reason for using triangular shaped is that the triangular cell placement in the reduction tree technique has a shorter wire length. In the paper design and implementation of conventional 8 bit Baugh Wooley multiplier algorithm has done and compared the result obtained with the new design of 8 bit Baugh Wooley multiplier algorithm using HPM reduction tree [6]. The comparative analysis has been done to prove that the new Baugh Wooley multiplier design is faster than the conventional design. The algorithm for Baugh Wooley multiplier is shown in Fig 1.

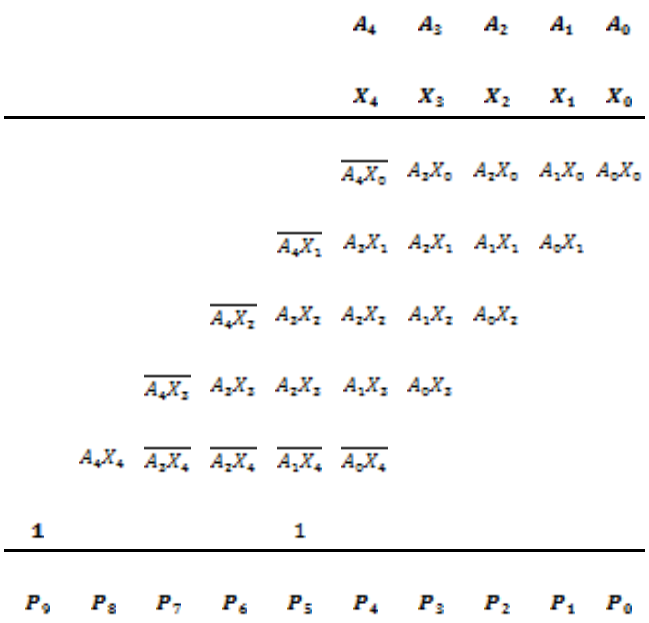

Fig. 1 Illustration of 5 bit Baugh Wooley Multiplier Algorithm

II. BAUGH WOOLEY MULTIPLIER

The Baugh-Wooley multiplication is one of the efficient methods to handle the sign bots. This approach has been developed in order to design regular multipliers, suited for 2's complement numbers [2]. Let two n-bit numbers, multiplier (A) and multiplicand (B), to be multiplied. A and B can be represented as

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i \qquad (1)$$

$$B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i \qquad (2)$$

Where the a_i's and b_i's are the bits in A and B, respectively, and a_{n-1} and b_{n-1} are the sign bits. The product, P = A x B, is given by the equation:

$$\begin{aligned} P &= A \times B \\ &= \left(-a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i\right) \times \left(-b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i\right) \\ &= a_{n-1}b_{n-1}2^{2n-2} + \sum_{i=0}^{n-2} a_i 2^i \sum_{j=0}^{n-2} b_j 2^j - 2^{n-1}\sum_{i=0}^{n-2} a_i b_{n-1} 2^i \\ &\quad - 2^{n-1}\sum_{j=0}^{n-2} a_{n-1} b_j 2^j \qquad (3) \end{aligned}$$

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The final product can be generated by subtracting the last two positive terms from the first two terms [2]. Instead of doing subtraction operation, it is possible to obtain the 2's complement of the last two terms and add all terms to get the final product. The last two terms are n-1 bits in which each that extend in binary weight from position 2^{n-1} up to 2^{2n-3}. On the other hand, the final product is 2n bits and extends in binary weight from 2^0 up to 2^{2n-1}. At first pad each of the last two terms in the product P equation with zeros to obtain a 2n-bit number to be able to add it with the other terms. Then the padded terms extend in binary weight from 2^0 up to 2^{2n-1} [3]. Let X is one of the last two terms that can represent it with zero padding as

$$X = -0 \times 2^{2n-1} + 0 \times 2^{2n-2} + 2^{n-1}\sum_{i=0}^{n-2} x_i 2^i + \sum_{j=0}^{n-2} 0 \times 2^j \qquad (4)$$

The final product [3], P = A x B becomes:

$$P = A \times B = a_{n-1}b_{n-1}2^{2n-2} + \sum_{i=0}^{n-2} a_i 2^i \sum_{j=0}^{n-2} b_j 2^j + 2^{n-1}\sum_{i=0}^{n-2} \overline{a_i b_{n-1}} 2^i + 2^{n-1}\sum_{j=0}^{n-2} \overline{a_{n-1} b_j} 2^j - 2^{2n-1} + 2^n \qquad (5)$$

Let A and B are 4-bit binary numbers, then the product [3], P = A x B will be 8 bit long and is

$$P = a_3 b_3 2^6 + \sum_{i=0}^{2} a_i 2^i \sum_{j=0}^{2} b_j 2^j + 2^3\sum_{i=0}^{2} \overline{a_i b_3} 2^i + 2^3\sum_{j=0}^{2} \overline{a_3 b_j} 2^j - 2^7 + 2^4 \qquad (6)$$

The block diagram for 4 bit Baugh Wooley multiplier is shown in Fig 2 and the detailed structure of each block has been shown in Fig3.

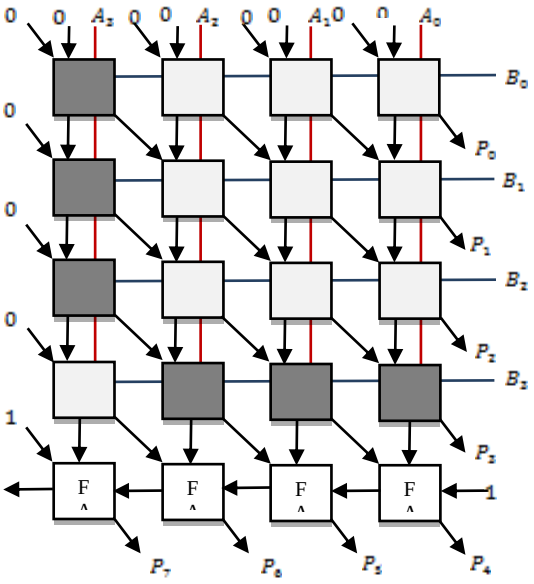

Fig. 2 Block Diagram of 4 bit Baugh Wooley Multiplier

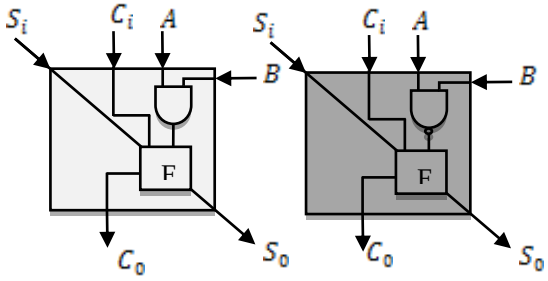

Fig. 3 Detailed View of White Cell and Grey Cell of the Baugh Wooley Multiplier

III. HPM BAUGH WOOLEY MULTIPLIER

The illustration of Baugh Wooley algorithm is represented in Fig 1. It is based on Hatamian's scheme [4]. It can be divided into three steps:

1) The most significant bit (MSB) of the partial-products in each N-1 rows and all bits of the last partial-product row, except its MSB, are inverted in the Baugh Wooley algorithm.
2) To the N^{th} column a '1' is added.
3) In the final result the MSB of it is inverted [6].

Implementation of Baugh Wooley multiplier using HPM method [6] is simply a straight forward method which is as represented in the algorithm. The partial products can be calculated using AND gates and the inverted products can be calculated using NAND gates. Insertion of '1' and the partial products are shown in Fig 3 that the block diagram for 8 bit Baugh Wooley multiplier using HPM [5]. The half adder and full adder cell of the High Performance multipliers explained in Fig 4 [1].

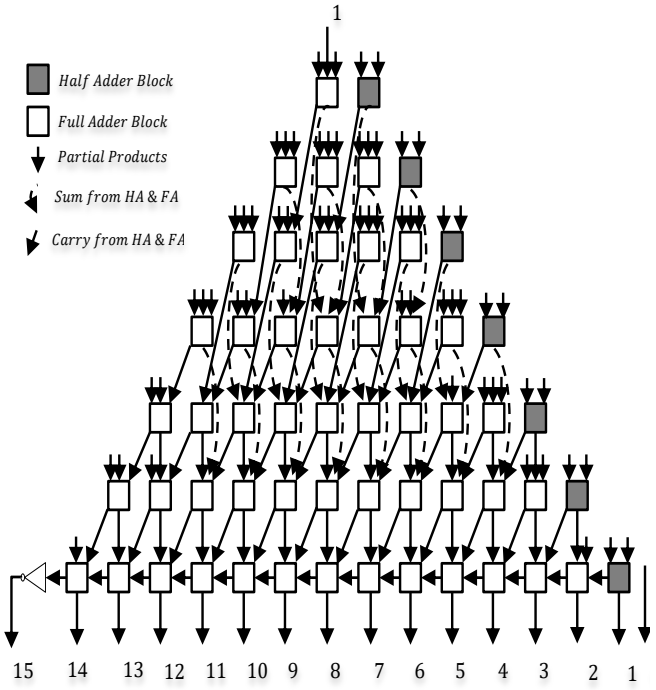

Fig. 4 Block Diagram for 8 bit HPM Baugh Wooley Multiplier.[6]

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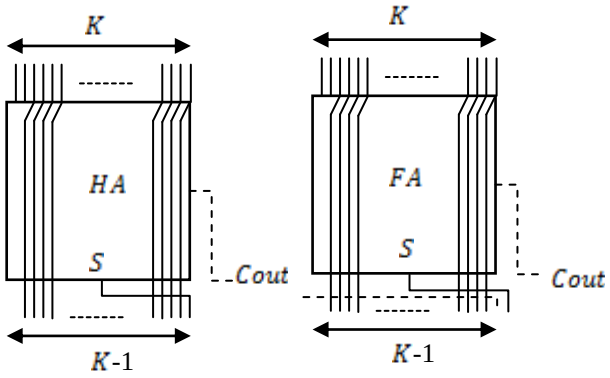


Fig. 5 HPM Half Adder and Full Adder Cell

IV. Simulation Results

A. Simulation Results of 8 bit Conventional Baugh Wooley Multiplier Using Cadence RTL complier 180nm process technology.

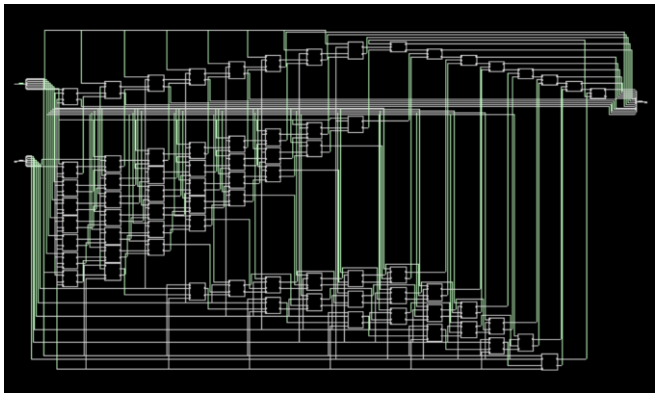
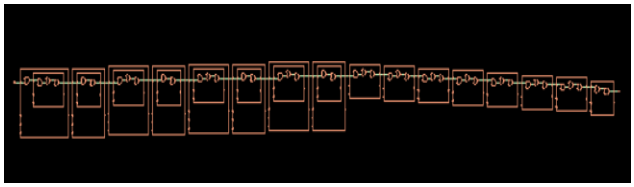


Fig. 6 RTL View of 8 bit Conventional Baugh Wooley Multiplier

Fig. 7 Worst Case Path of 8 bit conventional Baugh Wooley Multiplier



B. Simulation Results of 8 bit HPM Baugh Wooley Multiplier Using Cadence RTL complier 180nm process technology.

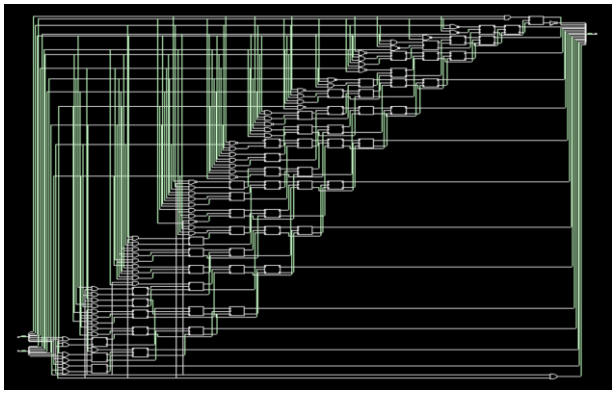


Fig. 8 RTL View of 8 bit HPM Baugh Wooley Multiplier

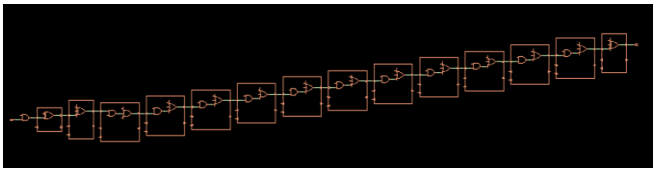


Fig. 9 Worst Case Path of 8 bit HPM Baugh Wooley Multiplier

V. Comparative Analysis

Comparison of conventional Baugh Wooley and HPM Baugh Wooley multiplier in terms of PDP, power, delay and area footprint.

Table 1 Synthesis Results of Conventional Baugh Wooley and HPM Baugh Wooley Multipliers in Cadence RTL

	Conventional Baugh Wooley	HPM Baugh Wooley
Leakage Power (nw)	7420.32	5344.02
Net Power (nw)	8177.19	7606.76
Internal Power (nw)	33895.62	31012.44
Switching (nw)	41504.38	39189.62
Data path Area	1479.64	1156.48
Number of Cells	137	121
Delay (ps)	3412.7	2704.6
PDP	2.79063E-14	2.05732E-14

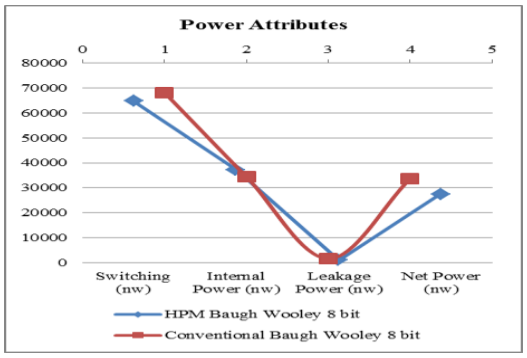


Fig. 10 Chart Representing Comparison of Power Attributes

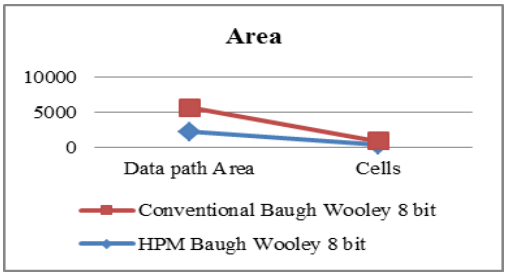


Fig. 11 Chart Representing Comparison of Data Path Area and Number of Cells

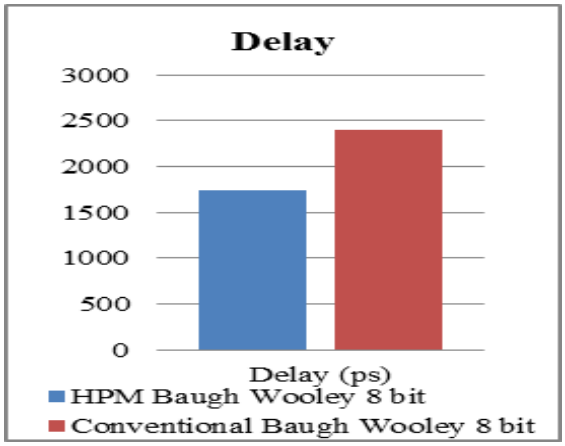


Fig. 12 Chart Representing Comparison of Delay

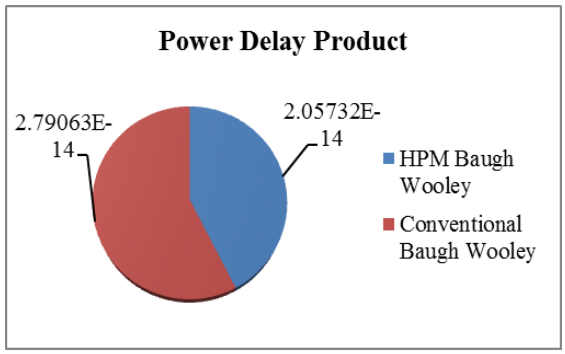


Fig. 13 Chart Representing the Power Delay Product

VI. CONCLUSION

By comparing the conventional Baugh Wooley with the HPM Baugh Wooley it is clear that the Baugh Wooley multiplier using HPM reduction tree is better than the conventional design. So high speed, low power, less delay and small area HPM Baugh Wooley multiplier can be used in high performance system.

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REFERENCES

1. H. Eriksson, P. Larsson-Edefors, M. Sheeran, M. Själander, D. Johansson, and M. Schölin, "Multiplier reduction tree with logarithmic logic depth and regular connectivity," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2006, pp. 4–8.
2. Pramodini Mohanty., "An Efficient Baugh-WooleyArchitecture forBothSigned & Unsigned Multiplication" International Journal of Computer Science & Engineering Technology (IJCSET) Vol. 3 No. 4 April 2012.
3. Steve Hung-Lung Tu., Chih-Hung Yen., "A High-Speed Baugh-Wooley Multiplier Design Using Skew-Tolerant Domino Techniques" IEEE 2006.
4. M. Hatamian, "A 70-MHz 8-bit x 8-bit Parallel Pipelined Multiplier in 2.5-µm CMOS," IEEE Journal on Solid-State Circuits, vol. 21, no. 4, pp. 505–513, August 1986.
5. M. Själander, H. Eriksson, and P. Larsson-Edefors, "An efficient twin-precision multiplier," in Proc. 22nd IEEE Int. Conf. Comput. Des., Oct.2004, pp. 30–33.
6. M. Själander and P. Larsson-Edefors, "The Case for HPM-Based Baugh-Wooley Multipliers," Department of Computer Science and Engineering, Chalmers University of Technology, Tech. Rep. 08-8, March 2008.
7. http://www.sjalander.com/research/multiplier
8. Magnus Själander., Per Larsson-Edefors., "High-Speed and Low-Power Multipliers Using the Baugh-Wooley Algorithm and HPM Reduction Tree." February 2008.
9. Joshin Mathews Joseph., V.Sarada., "Reconfigurable High Performance Baugh-Wooley Multiplier for DSP Applications" ITSI Transactions on Electrical and Electronics Engineering (ITSI-TEEE), ISSN (PRINT) : 2320 – 8945, Volume -1, Issue -4, 2013
10. Jin-Hao Tu., Lan-Da Van., "Power-Efficient Pipelined Reconfigurable Fixed-Width Baugh-Wooley Multipliers" IEEE Transactions On Computers, Vol. 58, No. 10, October 2009.
11. M. Sjalander and P. Larsson-Edefors, "High-speed and low-power multipliers using the Baugh-Wooley algorithm and HPM reduction tree," 15th IEEE International Conference on Electronics, Circuits and Systems, 2008.
12. M.V.P. Kumar, S. Sivanantham, S. Balamurugan, and P.S. Mallick, "Low power reconfigurable multiplier with reordering of partial products," International Conference on Signal Processing, Communication, Computing and Networking Technologies (ICSCCN), 2011.
13. V.B. Dandu, B. Ramkumar, and H.M. Kittur, "Optimization of hybrid final adder for the high performance multiplier," Third International Conference on Computing Communication & Networking Technologies (ICCCNT), 2012.

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