Explicit Pulse Triggered Flip Flop Design based on a Signal Feed-Through Scheme

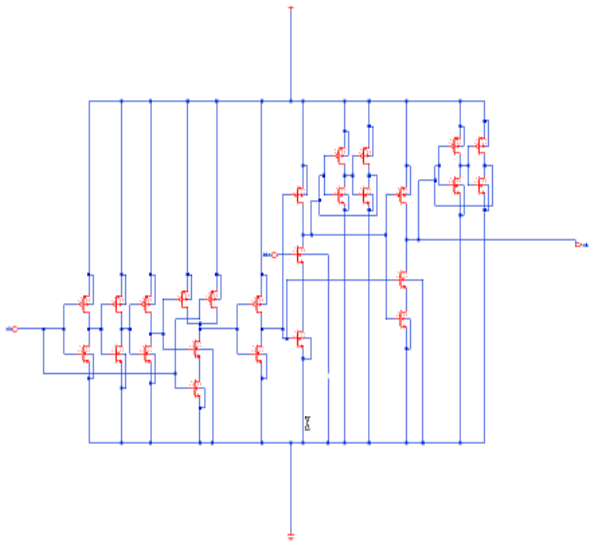
Jyothi Bandi, K. Rakesh

Abstract*— In this paper, a new explicit pulse triggered flip-flop (P-FF) design is implemented and simulated in GENERIC-TDK 130-nm technology. This explicit pulse triggered flip flop consist of a pulse generator and a true single phase clock latch based on a signal feed through scheme. The pulse generator is built with two CMOS inverters along with transmission gate logic which reduces the complexity of the circuit. The Pulse generation logic used in the explicit mode by a single pulse generator is shared for many number of flip flop at a time result in reduction of power not only this overall transistor count and delay can also been reduced. The transistor count has been reduced from 24 transistors to 16 transistors and power dissipated is 21.2133u watts. And this flip flop can achieve better D-Q delay and by using this explicit pulse triggered flip flop a synchronous counter is constructed and power dissipated is very less i.e. 19.928 nwatts.

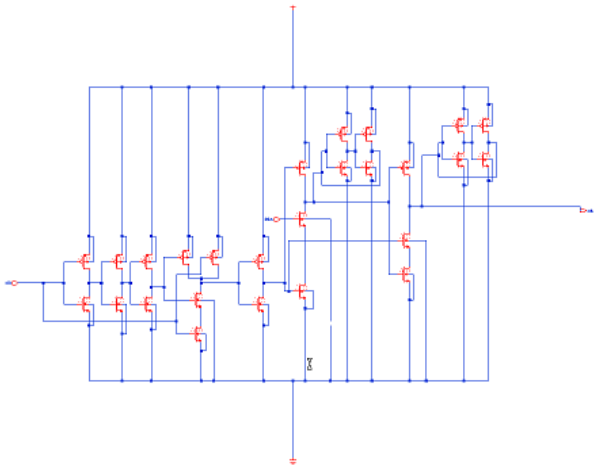
Keywords*— flipflop , to reduce no:of transistor , delay, power

I. INTRODUCTION

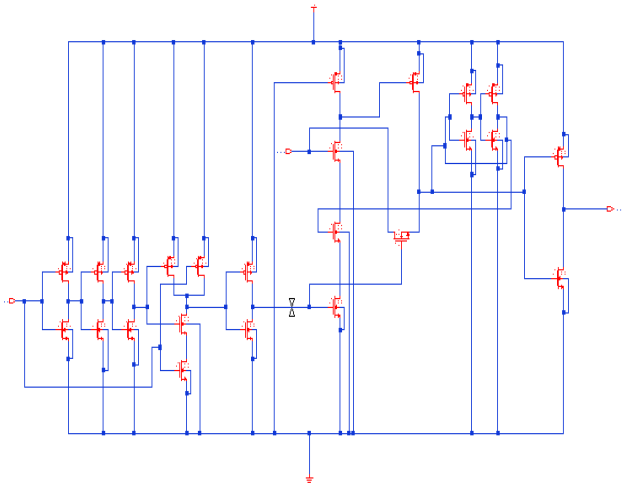
In current scenario the requirement of portable equipment is increasing rapidly so that development of VLSI design places a major role in the complex systems. Where the complex system consists of analog, digital as well as memory elements. Where all this can be integrated on a single chip. For designing a circuit we come across many design metrics like low power, high speed and reduced the area of chip by considering the above design metrics a novel explicit Pulse triggered flip flop is designed. Flip flop are extensively used as a basic storage elements in a digital systems. There are many type of flip flop designed basing of their operation like master and slave based flip flop, conventional transmission gate flip flop and pulse triggered based flip flop. In this design a pulse triggered flip flop is preferred compare with other two flip flop because pulse triggered flip flop is one which can execute in a single stage instead of two stages and sometimes the pulse triggered flip flop acts like an edge- triggered flip flop when there is a sufficient narrow latch is present. Pulse triggered flip flops are classified into two types based on their pulse generator used .They are implicit and explicit type pulse triggered flip flops. In implicit type of pulse triggered flip flop the pulse generator is present inside the flip flop where as in the explicit pulse triggered flip flop the pulse generator is present outside the flip flop [1], [2]



(a)



(b)



(c)

Manuscript Received on November 2014.

Jyothi Bandi, Department of Electronics and Communication Engineering, M.V.G.R. College of Engineering Vizianagaram, India.

K. Rakesh, Department of Electronics and Communication Engineering, M.V.G.R. College of Engineering Vizianagaram, India.

Fig. 1. Flip Flop Design (a) ep-DCO , (b) CDFF and (c) Base Paper Model Flip Flop

A. Some Explicit Type Pulse Triggered Flipflop

In this paper I have took some flip flop which exist already these designs are done in 130n meter technology and compare with other design which are done by changing the pulse generator fig 1(a) shows a classic explicit pulse triggered flip flop . In this design pulse generator is designed in a such way that four inveters are taken along with a Nand gate and a tspc latch.This design face a problem of switching power dissipation .To over come this problem another flip flop is designed . fig 1(b) show that CDFF design in this same type of pulse generator is taken by little change in the latch design .By keeping the problem in the mind a new design of CDFF is designed with some of the remedial measure like conditional precharge,conditional capture and conditional discharge and conditional pulse enhancement scheme have been proposed [3],[4],[5],[6],[7] to over come the problem of above design in the CDFf an extra transistor of nmos is taken and given to the Q-fdbk which controls the discharge and make the input data remains constant but this design face a problem of worst delay so to over come this problem another pulse triggered flip flop is designed .First a weak pmos transistor is taken and gate of pmos transistor is is connected to the ground and second a nmos pass transistor is used whichcontrolled by the pulse clock is included so that input data can drive node. The node level can thus be quickly pulled up to shorten the data transition delay [8]

II. PROPOSED MODEL

A novel explicit pulse triggered flip flop is designed. This flip flop consist of a pulse generator and a transmission gate .this new explicit pulse triggered flip flop works on three stages i.e. pulse generator, latch and a bistable element.

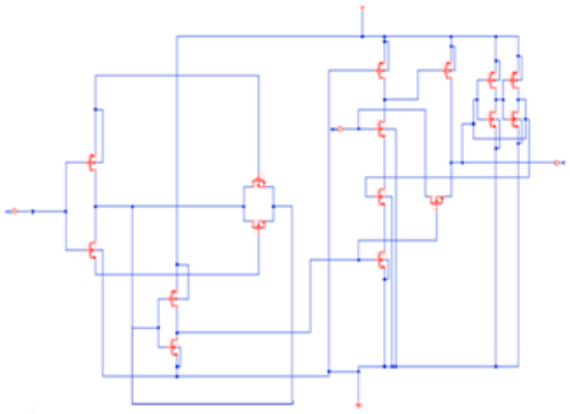


Fig.2. Schematic of the New Flip Flop Design

Fig 2 shows a latch which consider with a nmos pass transistor and weak pmos transistor to over come the problem of fliping of the output.

Principle working: -

Stage1: when clock is given as input to the first CMOS inverter and its output is given as a input to the transmission gate and the out of it is given as the input of the second CMOS inverter and its output is the pulse generator output. his pulse generator generates the pulse and it is given to the latch.

Stage2: when the pulse generator gives 1 as input to the latch .since the latch consists of pmos and nmos transistors and when it is given '1' then all pmos transistors are in off state i.e. non conducting and the nmos transistors are in on state so it passes the data which applied to it .since the data input is signally feed through to the pass transistor.

Stage3: this stage consists of a bistable element which stores the data. Since this bistable element is also called regenerator property. When clock is '0' then all the nmos transistors are in off state and pmos transistors are in on state .these transistor retrieve whatever data present in bistable element as a output.

III. APPLICATION

By using a explicit pulse triggered flip flop a Synchronous counter with 3 bits is designed as shown in fig 3.which can be expanded to 4,8,12 and 16 bit.

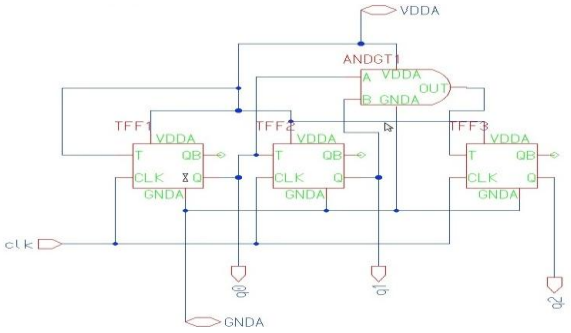


Fig. 3. Schematic of a 3-bit Synchronous Counter of Proposed Flip Flop

IV. SIMULATION RESULTS

The proposed pulse triggered flip fliop is designed against existing flipflop design and this design is designed in GENERIC 130n meter technology and simulated both in pre-layout and post-layout simulation . after simulation delay ,number of tansistor and power is less compare to existing flip flop this is shown in table1 and fig 4 shows waveform of new explicit pulse triggered flip flop and fig 5 shows layout of it. And fig 6 shows waveform of synchronous counter and fig 7 shows layout it.

Table1
Comparison of flipflop design

PARAMETERS	EXISTING MODEL	PROPOSED MODEL
DELAY	9.45ns	1.4ns
NO:OF TRANSISTOR	24	16
LAYOUT AERA	69.13um^2	45.13um^2
POWER DISPATION	21.24 u watts	478.66p watts

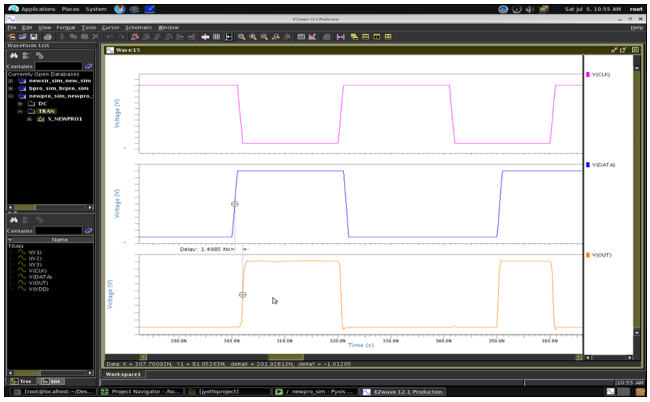


Fig. 4. Simulation Waveform

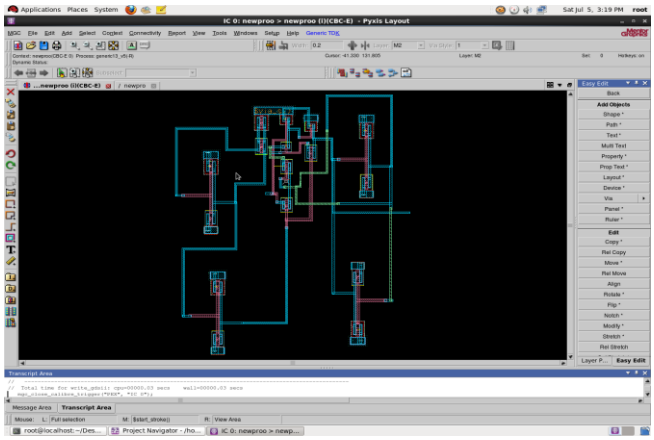


Fig. 5. Layout of New Flipflop

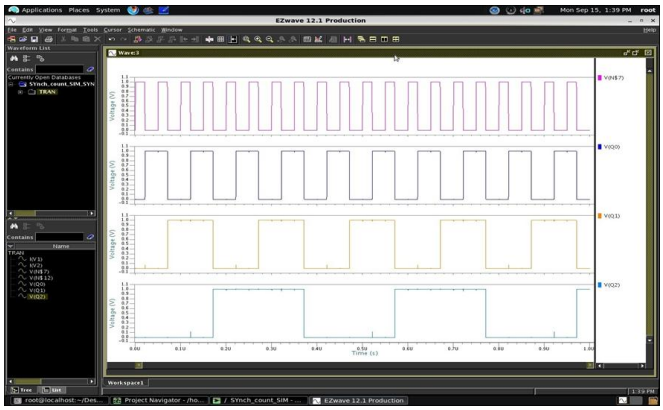


Fig. 6. Waveform of a 3-Bit Synchronous Counter of Proposed Flip Flop

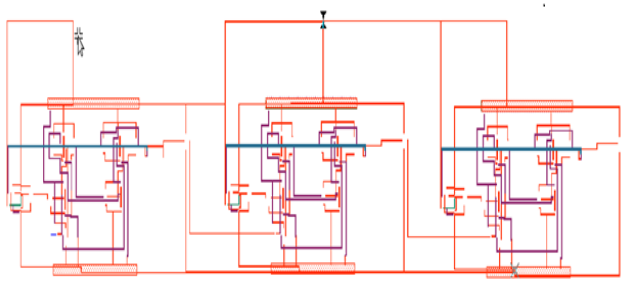


Fig. 7. Layout of a 3-Bit Synchronous Counter of Proposed Flip Flop

V. CONCLUSION

A novel explicit pulse triggered flip flop is designed in such a way that the pulse triggered flip flop is designed using two CMOS inveter and a transmission gate along with a tspc(true signal pulse clock) latch . This novel flip flop is mainly forced on reduction of no:of transistor ,delay , layout area as well as power dispation compare to existing flip flop design.

REFERANCES

[1] Xia W.Q.shui,X.Y and Yao, W.L "Dual-vth based double-edge explicit-pulseed level-converting flip-flop" in IEEE-International Conference on Electronics ,communications and control (ICECC),(2011)

[2] Bhargavaram,D.and Pillai,M.,"low power dual edge triggered flip-flop".in Advance in Engineering,science and Management (ICAESM),International Conference on IEEE,(2012),63-67.

[3] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.

[4] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional pre charge techniques for power-efficient dual-edge clocking," in *Proc. Int. Symp. Low-Power Electron. Design*, Aug. 2002, pp. 56–59.

[5] P. Zhao, T. Darwish, and M. Bayoumi, High-performance and low power conditional discharge flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 477–484, May 2004.

[6] M.-W. Phyu, W.-L. Goh, and K.-S. Yeo, "A low-power static dual edge triggered flip-flop using an output-controlled discharge configuration," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 2429–2432.

[7] Y.-T. Hwang, J.-F. Lin, and M.-H. Sheu, "Low power pulse triggered flip-flop design with conditional pulse enhancement scheme," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 2, pp. 361–366, Feb. 2012.

[8] Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme *IEEE transactions on very large scale integration (VLSI) systems, vol. 22, no. 1, january 2014*