Comparative Analysis and Study on 4-bit RCA and CSK using CMOS Logic

Suhel Ranjan Mondal, Monalisa Bhowmik, Santanu Maity, Razia Sultana

***Abstract*— Adders are the most basic and essential component used in Digital signal processing and is widely used in the digital integrated circuits. In VLSI application area, delay and power are the important factors which must be taken into account in design of a full adder. In this paper a comparative analysis in terms of speed, power consumption and area and PDP for design of 4 bit RCA and CSK is compared by CMOS logic style , quantitatively and qualitatively by performing detailed transistor level simulation using T spice v13.0.**

***Index Terms*—Ripple carry Adder, Carry Skip Adder, ,full adder, high speed, low power.**

I. INTRODUCTION

Adders are the building block in DSP applications. Adders perform operations like Addition, Subtraction, Multiplication and Division. Chen et. Al found that addition is the most frequently operation in the Digital signal processing [1]. The key component in DSP is the binary adder and the basic unit on which every binary adder structure is based, is the Full adder cell. Full adder cell contains the three inputs A, B and C_{in} and two outputs - sum **S** and Carry $\mathbf{C_{out}}$. By cascading the full adder cells, we have the basic Adder structure called as "Ripple carry adder" in which "n" full adder cells are cascaded to get the n - bit Ripple carry adder and carry generated at n_{th} bit is given as the input to the n+1 bit in addition to the A and B inputs. As Ripple carry adder is the most basic one among the other adders but also slowest of them all, because of the propagation of the carry from LSB to MSB. Ripple carry adder is slowest among all the adder structure because of the rippling of the carry. Carry look Ahead adder solves the problem of carry propagation from right to left by using carry propagate and the carry generate signals for reducing delay but the area, number of gates is increased and thus complexity of the system is increased. In Carry skip adder, the propagation time of carry is reduced by skipping over the group of adder stages and presents hardware and performance compromise.

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II. LITERATURE SURVEY

Much of the research efforts of the past years in the area of digital electronics have been directed towards increasing the speed of digital system. Recently the requirement of portability and the moderate improvement in battery performance indicates that the power dissipation is one of the most critical design parameter. The three most widely accepted metrics to measure the quality of a circuit or to compare various circuit styles are area, delay and power dissipation. Portability imposes a strict limitation on power dissipation while still demands high computational speeds. Hence, in recent VLSI Systems the power-delay product becomes the most essential metric of performance. The reduction of the power dissipation and the improvement of the speed require optimizations at all levels of the design procedure. Since, most digital circuitry is composed of simple and/or complex gates; we study the best way to implement adders in order to achieve low power dissipation and high speed. A detailed review of the existing CMOS circuit design styles and Reversible logic style is given, describing their advantages and limitation. Also, various design and implementation of Carry Skip Adder were analyzed in the terms of delay and power consumption using T-Spice.
Conventional Static CMOS has been a technique of choice in most Processor design. Alternatively, Static Pass Transistor circuit has also been suggested for Low Power applications [2]. Dynamic circuit, when clocked carefully, can also be used in Low Power, High speed Systems [3].

III. LOGIC DESIGN STYLES

The increasing demand for low-power VLSI can be addressed at different steps of VLSI design cycle, such as the architectural, circuit, layout, and the process technology level. At the circuit design step, considerable potential for power savings exists by means of proper choice of a logic style for implementing circuits. This is because all the important parameter governing power dissipation-switching capacitance, transition activity, and short-circuit currents—are strongly influenced by the chosen logic style. Depending on the application, circuit can be implemented in different logic style.

A. STANDARD CMOS LOGIC

It is the most common and widely utilized digital logic in almost any application field. Still, other digital logic styles exist and are utilized in the industry as well. Since we aim in this thesis work for special design characteristics, such as very low

power consumption and very small sized designs, it is fair to have a look at other digital logic design styles as well. The schematic diagram of a conventional static CMOS full adder cell is illustrated in figure 1.The signals noted with '-' are the complementary signals. The p-MOSFET network of each stage is the dual network of the n-MOSFET. First the fundamental differences between static and dynamic logic will be explained.[4]

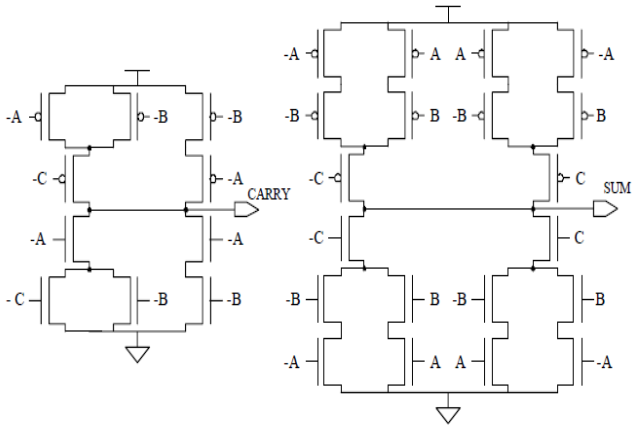

Fig. 1 CMOS Logic Full Adder.

IV. IMPLEMENTATION OF 4-BIT RIPPLE CARRY ADDER

The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. A number of full adders may be added to the ripple carry adder or ripple carry adders of different sizes may be cascaded in order to accommodate binary vector strings of larger sizes. For an n-bit parallel adder, it requires n computational elements (FA). Figure below shows an example of a parallel adder: a 4-bit ripple-carry adder. It is composed of four full adders. The augends' bits of x are added to the addend bits of y respectfully of their binary position. Each bit addition creates a sum and a carry out. The carry out is then transmitted to the carry in of the next higher-order bit. The final result creates a sum of four bits plus a carry out (c4).[5]. In this carry out of previous full adder becomes the input carry for the next full adder. It calculates sum and carry according to the following equations. As carry ripples from one full adder to the other, it traverses longest critical path and exhibits worst case delay.

$S = Ci \text{ XOR } (Ai \text{ XOR } Bi)$

$Cout = AiBi + Ci (Ai \text{ XOR } Bi)$ where i=0,1,2,3…….

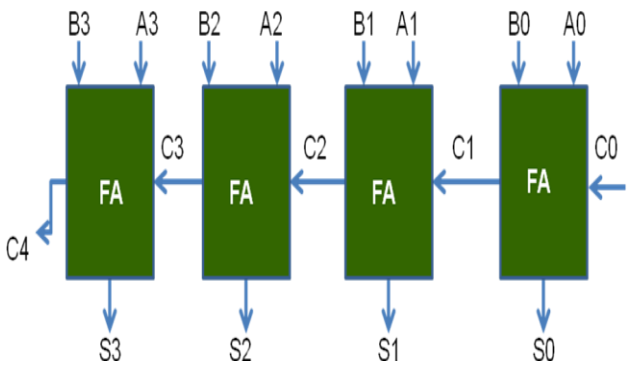

Fig. 2 Architectural block diagram of 4-bit Ripple Carry Adder

The implementation of 4-bit ripple carry adder using CMOS Logic is shown in Fig.3 and its corresponding simulated waveform in Fig. 4.

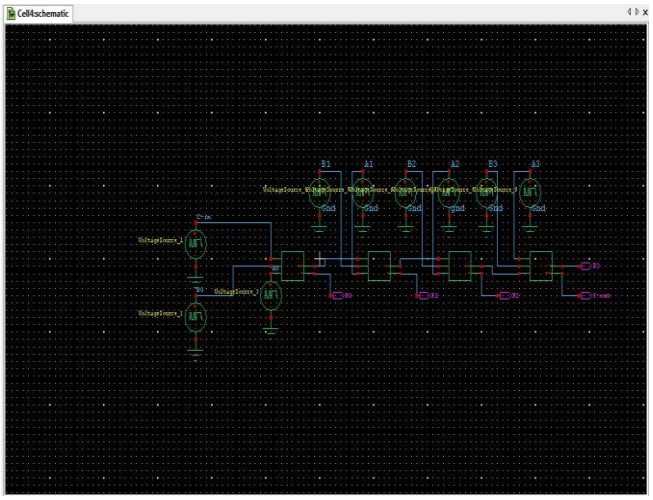

Fig. 3 Schematic diagram of Full Adder by CMOS logic

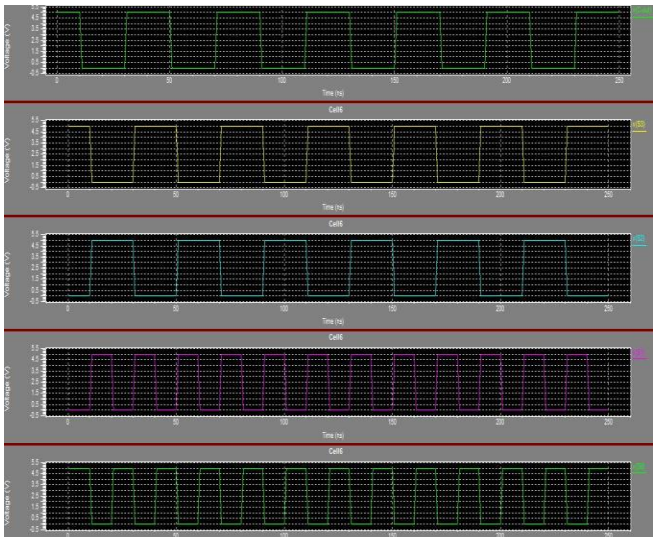

Fig. 4 Output waveform of 4 –bit Ripple Carry Adder by CMOS Logic

V. ARCHITECTURE OF CARRY SKIP ADDER

The carry skip adder provides a compromise between a ripple carry adder and a CLA adder. The carry skip adder divides the words to be added into blocks. Within each block, ripple carry is used to produce the sum bit and the carry. The Carry Skip Adder reduces the delay due to the carry computation i.e. by skipping over groups of consecutive adder stages [6]. • If each Ai # Bi in a group, then we do not need to compute the new value of Ci+1 for that block; the carry-in of the block can be propagated directly to the next block. • If Ai = Bi = 1 for some i in the group, a carry is generated which may be propagated up to the output of that group. • If Ai = Bi = 0, a carry, will not be propagated by that bit location. The basic idea of a carry-skip adder is to detect if in each group all Ai # Bi and enable the block's carry-in to skip the block when this happens as shown in figure1. In general a block-skip delay can be different from the delay due to the propagation of a carry to the next

bit position [7][8]. With carry skip adders, the linear growth of carry chain delay with the size of the input operands is improved by allowing carries to skip across blocks of bits, rather than rippling through them.

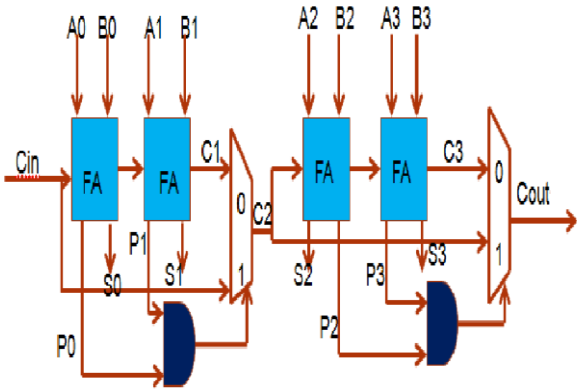

Fig. 5 Architectural block diagram of 4-bit CSKA

The implementation of 4-bit CSKA using CMOS Logic is shown in Fig. 6 and its corresponding simulated waveform in Fig.7.

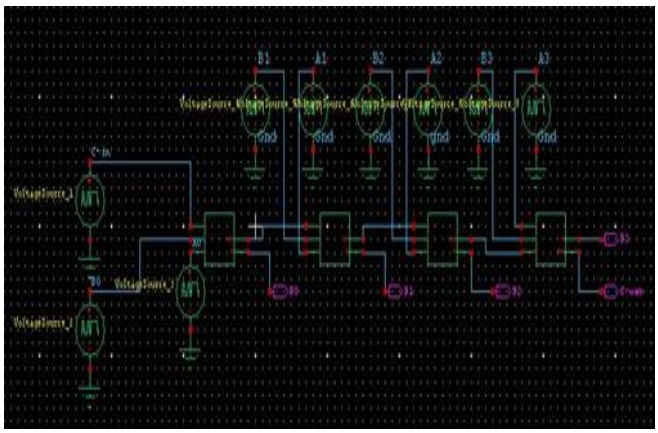

Fig. 6 schematic diagram of CSKA using CMOS Logic

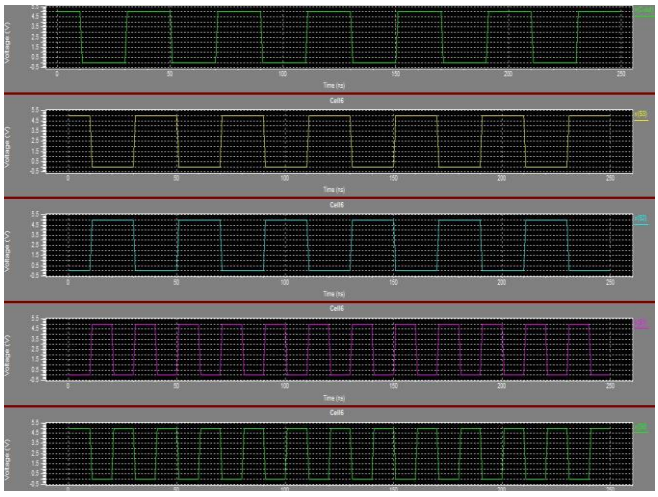

Fig. 7 Simulated waveform of CSKA using CMOS Logic

VI. PERFORMANCE PARAMETERS AND SIMULATION SETUP

The 4-bit Carry Skip Adder is compared based on the performance parameters like propagation delay, number of transistors and power dissipation. To achieve better performance, the circuits were designed using Static CMOS logic process technology and Reversible logic process. The channel width of the transistors is 450n for the NMOS and 900n for the PMOS and the channel length is 150n with Vdd 1 volt. All the circuits have been designed using TANNER EDA with Model file as dual.md. direct simulation method is used to analyze the result.

Table. 1 shows Comparative Experimental results of RCA and CSK using CMOS logic in terms of area, power and delay.

ADDER	NO. OF TRANSISTOR	POWER DISSIPATION (mw)	DELAY (ns)	PDP (PJ)
RCA	112	.0929	11.39	1.058
CSKA	130	0.032	10.77	.3446

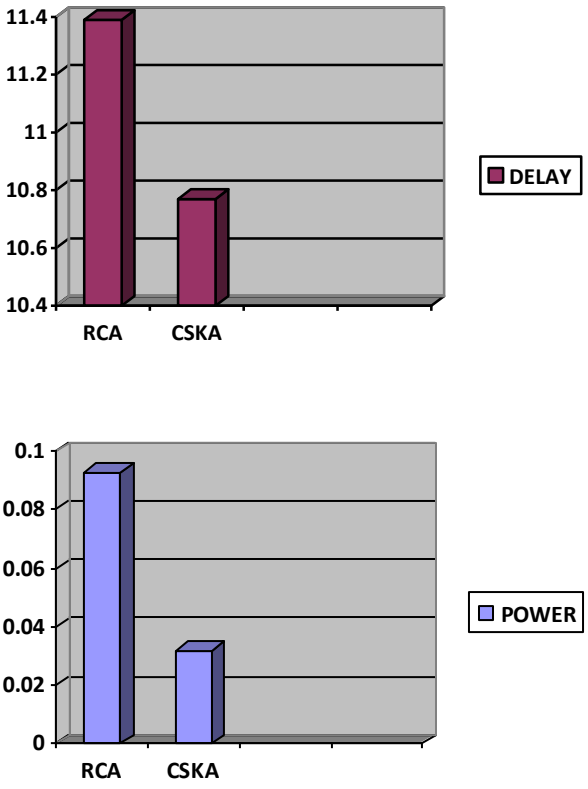

Fig. 8. Comparison between RCA and CSKA in term of delay and Power dissipation.

VII. RESULT ANALYSIS

It has been observed that Carry Skip Adder (CSK) exhibit better characteristics (speed and Low-Power) as compared to Ripple Carry Adder (RCA). So, Carry Skip Adder can be used where portability and high speed is the prime aim. Where Carry Skip Adder, (CSK) consumes the lowest power and delay. . With the reduction of propagation delay by skipping the group of adder stages, it can be considered best Adder among the two with respect to all parameters of 4-bit Carry Skip Adder architectures.

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VIII. CONCLUSION

Use of Logical Effort delay model for performance comparison of two different adder architecture were presented . Simulated results show that optimization based on logical effort reduces the delay and power in both the adder architecture carry skip adder and ripple carry adder.

IX. ACKNOWLEDGMENT

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