A Comparative Study: Multiplier Design using Reversible Gates logic

I. Thahirabanu, A. Ananthi, G. Vishnupriya, G.Usha

Abstract---*In this paper we propose a new concept for multiplication by using modified booth algorithm, booth multiplier & wellece tree multiplier and reversible logic function. By combining modified booth algorithm with reversible gate logic it will produces further less delay compare to all other. Addition subtraction operation are realized using reversible DKG gate. Reversible logic circuits have theoretically zero internal power dissipation because they do not lose information, the classical set of gates such as AND, OR, and XOR are not reversible. This modified booth multiplier, modified booth multiplier & wellece tree multiplier with reversible gate logic are synthesized and simulated by using Xilinx 13.2 ISE simulator.*

Keywords ---Reversible logic gates, reversible logic circuit, partial products, adder, multiplier, power analysis, quantum computing, Future computing, simulation outputs.

I. INTRODUCTION

One of the major goals in VLSI circuit design is reduction of power dissipation and to improve system performance. Multiplication algorithms have considerable effect on processors performance. As demonstrated by R. Landaulet in the early 1960s, irreversible hardware computation, regardless of its realization technique, results in energy dissipation due to the information loss [1]. Hence In 1973, Bennett showed that in order to avoid KTln2 joules of energy dissipation in a circuit, it must be built using reversible logic gates [2]. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector Such gates or circuits allow their production of the inputs from observed outputs and we can determine the inputs from the outputs [3-5]. A reversible logic circuit.

In 1965, according to 'Moore's law', stated by Gordon Moore, Intel Co-founder, the performance of integrated circuits improve at an exponential rate with the performance per unit cost increasing by a factor of 2 every 18 months. This resulted in shrinking the dimensions on integrated structures to make it possible to operate at higher speed for the same power per unit area [1] One should not forget that there is a minimum of quantum energy associated with elementary events which puts a fundamental limit on the miniaturization. So the question is, will Moore's law going to end?

Revised Version Manuscript Received on August 30, 2015.

I. Thahirabanu, Department of Electronics and Communication Engineering, SNS College of Technology, Coimbatore, Tamil Nadu. India.

A. Ananthi, Department of Electronics and Communication Engineering, SNS College of Technology, Coimbatore, Tamil Nadu. India.

G. Vishnupriya, Department of Electronics and Communication Engineering, SNS College of Technology, Coimbatore, Tamil Nadu. India.

G. Usha, Department of Electronics and Communication Engineering, SNS College of Technology, Coimbatore, Tamil Nadu. India.

Using current technology more and more components are getting packed onto the chip and at the same time the power dissipation in the present day computer is very high. So, one of the major current research trends is towards saving of the power. Later C. H. Bennett, in 1973, showed that in order to avoid KTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [3]. Reversible logic ensures zero information loss and low power dissipation. In the present work 4-bit multiplier circuit is constructed using the multi-control input Toffoli synthesis. Toffoli gate is an universal reversible gate and it is used very frequently for the synthesis of a reversible circuit compared to the other gate like Fredkin gate. To ffoli gate synthesis is known to result in a minimum cost circuit, a primary goal of optimization. The reversible logic circuit synthesized usually results in a circuit with higher cost. The reversible logic gates used for the construction of a circuit needs to be implemented using universal gates. This design is presented in this paper which is organized as follows: In Section 2 basic reversible logic gates are discussed. In section 3, the new reversible logic gate, BVPPG gate which is implemented using Toffoli gates is discussed. In Section 4, the design 4-bit multiplier using optimized reversible logic gates and its Toffoli synthesis is presented. In section 5 comparison of the design with the other existing designs is presented. Section 6 presents conclusions with scope for further research. In this design we use reversible logic gates[2] in the place of full adders to reduce the power and delay. A reversible logic circuit should have features like use minimum number of reversible gates[2], use minimum number of garbage outputs, use minimum

II. REVERSIBLE LOGIC GATES

A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits, Direct fan-out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. So an optimized design of a reversible logic circuit is very important to have the best cost metrics.

The important cost metrics [5] which are used to measure the performance of a reversible logic circuit is,

- Gate count-GC- The number of reversible gates used in circuit.
- Line count-LC- Number of circuit lines
- Quantum cost- QC - Cost of the circuit in terms of the cost of a primitive gate.
- Garbage outputs- GO - Number of unused outputs present in a reversible logic circuit

III. BASIC REVERSIBLE LOGIC GATES

A. Peres gate

A 3*3 Peres gate [8]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4. It is needs two Toffoli gates for its construction

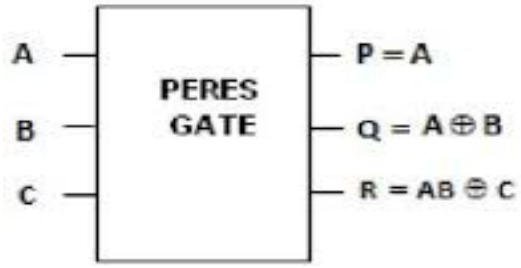

Fig.3.1.PG Gate

B. double Peres gate

The quantum cost of a DPG gate is calculated to be equal to 6 from its quantum realization.

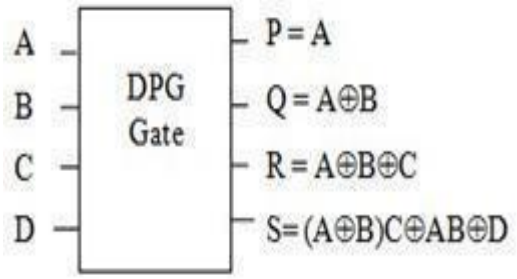

Fig. 3.2. DPG Gate

C. DKG gate

Reversible function is the main objective of the reversible logic theory. A 4* 4 reversible logic DKG[2] gate that can work uniquely as a reversible Full adder and a reversible Full subtractor. It can be verified that input pattern representing to a particular output pattern can be uniquely determined. If the input A=0, the proposed gate acts as a reversible Full adder DKG gate, and if input A=1, then it acts as a reversible Full subtractor DKG gate. It has been proved that at least the two garbage outputs are required by the reversible full-adder circuit to make the output combinations unique.

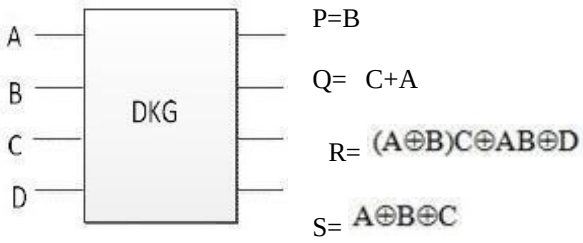

Fig.3.3 DKG Gate

D. MFA gate:

The purpose of this paper is the design of reversible multiplier circuits with the aim of optimizing its hardware complexity to make it more economical in terms of number of garbage outputs and constant inputs without losing its efficiency. The garbage outputs identified as the outputs which are not used in further computations and constant inputs need to realize only balanced functions. This is the driving force that makes the proposal of new reversible multiplier circuit uses the modified full adder (MFA) [17] as shown in Fig.3.4

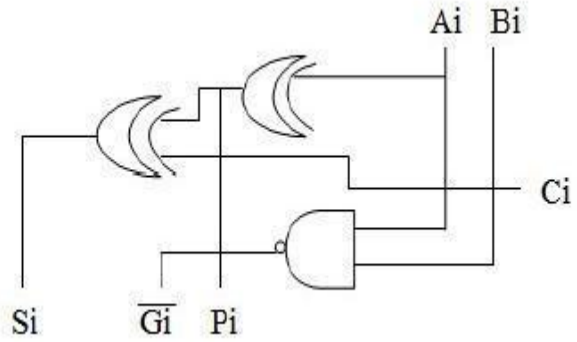

Fig. 3.4.MFA Gate

IV. DESIGN OF 4-BIT MULTIPLIER

A. booth multiplier

As proposed in [8], to implement an n operand addition circuit part a carry save adder (CSA) is used. The CSA tree reduces the four operands to two. Thereafter, a Carry Propagating Adder (CPA) adds these two operands and produces the final 8-bit product. The proposed four operand adder shown in the figure 13 uses DPG gate as a reversible full adder and Peres gate as half adder.

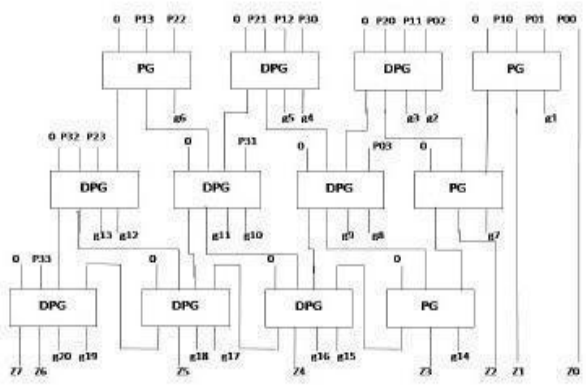

Fig.4.1 implementation of booth multiplier

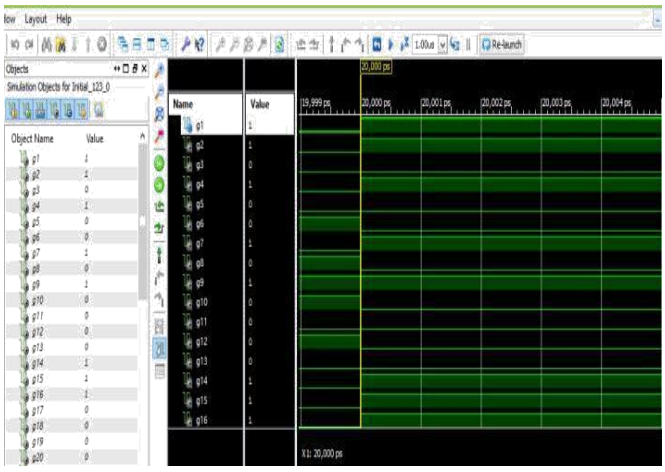

Fig.4.1.1 simulation of booth multiplier

B. modified booth multiplier

A Parallel adder/subtract or is an cascaded of full adders/sub tractors and inputs are simultaneously applied. The carry/borrow produced at a stage is propagated to the next stage. When the control input A=0, the circuit behaves as a parallel adder, generates a 4 bit sum and a carry out, as shown in Fig 4. If the control input A=1, the circuit behaves as a parallel subtractor, generates a 4 bit difference and a borrow out, as shown in Fig 5.

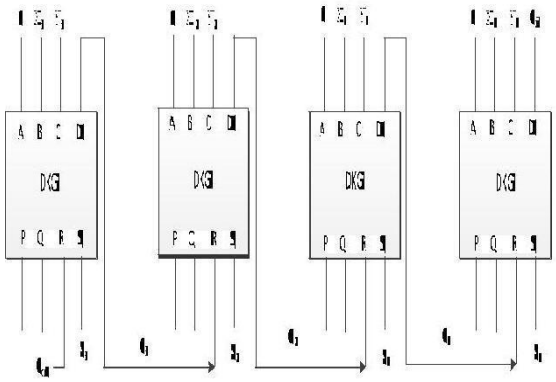

Fig.4.2 implementation of Modified booth multiplier

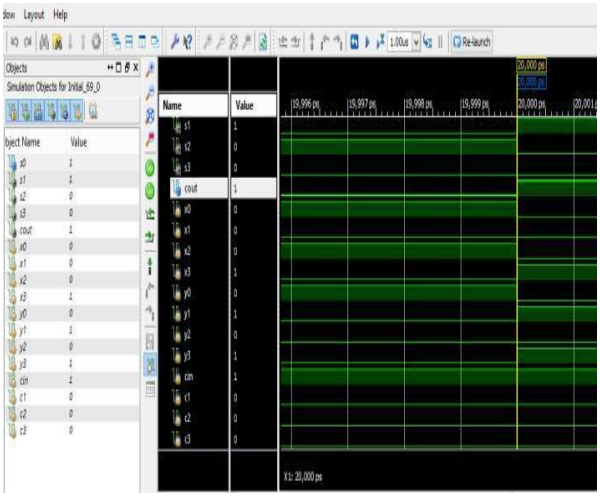

Fig.4.2.1. simulation of modified booth multiplier

V. WALLECE TREE MULTIPLIER

The RPA circuit as shown in Fig.3 needs reversible full adder (FA) and half adder (HA). Many reversible full adders have been proposed in the past.

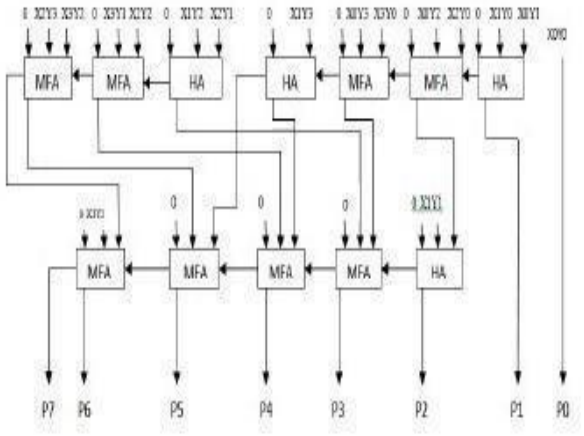

Fig.4.3 implementation of wallece tree multiplier

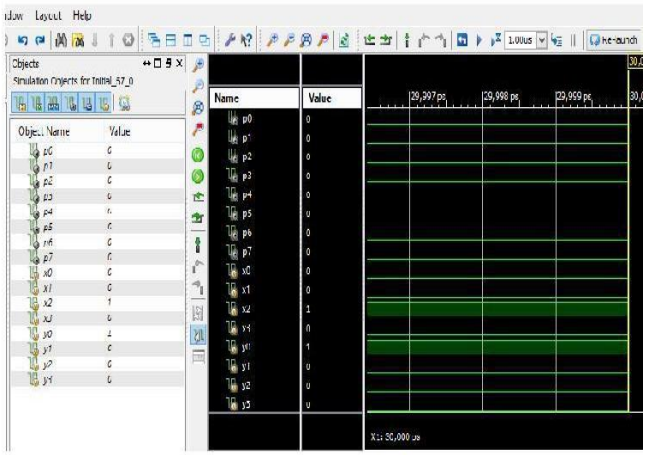

Fig.4.3.1. simulation of wallece tree

VI. CONCLUTION

Multiplier is a basic arithmetic cell in computer arithmetic units. Furthermore, reversible implementation of this unit is necessary for quantum computers. The focus of this paper is the application of a reversible logic gate to realize a 4-bit multiplier using a new reversible logic gate which is designed keeping in view the optimization factors of the reversible circuits and is synthesized using Toffoli synthesis. Toffoli gate circuits has been demonstrated as a promising alternative to achieve minimal reversible circuits than that achieved using heuristic synthesis approach namely the transformation-based method. a new MAC architecture to perform the multiplication-accumulation, To efficiently process the digital signal processing and multimedia application this architecture was proposed. the overall MAC performance has been improved By eliminating the independent accumulation process that has the greatest delay and merging it to the compression process of the partial products, almost twice as much as in the previous work and by replacing full adder in the CSA with reversible logic gate further improves the performance. Consequently, the proposed architecture can be used effectively where we requiring high throughput such as a real-time digital signal processing. Targeting this purpose, various designs can be found in the literature. The comparison between the all three proposed multiplier and those of the previous works showed that the garbage output, power consumption& delay time. The proposed hardware was implemented and synthesized through Xilinx ISE 13.2 tool.

Parameters	No of Garbage Output	Delay Time
Booth Multiplier	36	3.399ns
Modified Booth Multiplier	31	1.013ns
Wallece Tree Multiplier	20	1.927ns

Table. 1 Comparative Table

REFERENCE

1. Gordon E. Moore, “Cramming more components onto integrated circuits”, Electronics Volume 38, number 8, April 19, 1965

2. R. Landauer, "Irreversibility and heat generation in t he computing process," IBM Journal. Research and Development, vol. 3, pp. 183-191, July1961
3. C. H. Bennett, "Logical reversibility of computation," IBM J. Research and Development, pp. 525-532, November 1973.
4. DeBenedictis, E. Will Moore's Law be Sufficient? in proceedings of supercomputing, 2004. ANewVLSIArchitectureof
5. Parallel Multiplier–Accumulator Based on Radix-2 Modified Booth Algorithm "Young-Ho Seo, Member,IEEE,and Dong-Wook Kim, Member, IEEE
6. "A Distinguish Between Reversible And Conventional Logic Gates" B.Raghu Kanth, B.Murali Krishna Sridhar , V.G. Shanti Swaroop,
7. H. Thapliyal and M. B. Srinivas, "Novel reversible TSG gate and its application for designing reversible carry look ahead adder and other adder architectures", Proceedings of the 10th Asia-Paci_c Computer Systems Architecture Conference
8. M. Haghparast and K. Navi, "A Novel Reversible Full Adder Circuit for Nanotechnology Based Systems". Applied Sci., 7 (2007) 3995.
9. M. Haghparast and K. Navi, "Design of a novel reversible multiplier circuit using HNG gate in nanotechnology".
10. Fredkin, E. and T. Toffoli, 1982. Conservative logic. Int "l J. Theoretical Physics.

BIBLIOGRAPHY

I. Thahirabanu, is pursuing her III year , Electronics and Communication Engineering from SNS College of Technology, Coimbatore. Her area of interest is VLSI, LAB VIEW circuit designing and embedded system.

A. Ananthi, is pursuing her IV year, Electronics and Communication Engineering from SNS College of Technology, Coimbatore. Her area of interest is VLSI, LAB VIEW circuit designing and embedded system.

G. Vishnupriya, is pursuing her III year, Electronics and Communication Engineering from SNS College of Technology, Coimbatore. Her area of interest is circuit designing and embedded system.

G. Usha, is pursuing her III year, Electronic and Communication Engineering from SNS College of Technology, Coimbatore. Her area of interest is circuit designing and embedded system.