Design of Area and Speed Efficient Square Root Carry Select Adder Using Fast Adders

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Abstract: ***Area and speed are the most important design objectives in integrated circuits. As addition is the basic operation of all computer arithmetic, adders are one of the widely used components in digital integrated circuit design. Since propagation of carry is of major concern in designing efficient adders, this paper presents different fast adders and their performance analysis. Among all the adders discussed Square root Carry Select Adder (SQCSA) provides a good compromise between cost and performance. As, Conventional SQCSA is still area consuming due to dual Ripple Carry Adder(RCA)structures, modifications are done at gate level to reduce area. Modified SQCSA is designed using fast adders like Carry Skip Adder (CSA) and Carry Look-Ahead Adder (CLA) to increase the speed of operation.***

Keyword: - (SQCSA), (CLA), (CSA), Conventional, designed, Carry, Adder, concern, adders, Among, Modified

I. INTRODUCTION

In rapidly growing electronic industry, faster units are not only of concern for design but also smaller area and less power become major concerns for design of VLSI circuits. So a VLSI designer has to optimize area delay and power constraints for increasing portability and battery life of portable devices[1]. As we know millions of instructions per second are performed in micro processors speed of operation is the most important constraint to be considered while designing multipliers. These constraints are difficult to achieve so depending on application compromise between constraints has to be made. There are many ways to design adder [2]. The Ripple carry Adder (RCA) exhibits the most compact design but slowest in speed because for an N-bit RCA, the delay is linearly proportional to N[2]. Thus for large values of N the Ripple Carry Adder gives greater delay of all adders. An N-Carry Look-ahead Adder (CLA) gives fast results when compared to RCA for $N \leq 4$, but for large values of N its delay increases. The structure of Carry Select Adder is built using dual Ripple Carry Adders which increase area. In order to reduce the area and power Modified Carry Select Adder(MCSA) is implemented whereone ripple carry adder at each stage of addition is replaced with BEC (Binary to Excess-1 Converter)[1].To further increase the performance of MCSA the other RCA's are replaced with still faster adders like Carry Skip Adder and Carry Look-ahead Adders long.

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The results show a greater improvement in terms of delay and number of logic levels is reduced. The square-root carry select adder is constructed by equalizing the delay through two carry chains and the block multiplexer signal from previous stage[.3] It is also called as non-linear carry select adder. The existing modified SQRT CSLA uses Binary to Excess-1Converter (BEC) instead of RCA with Cin-=1 to achieve lower delay and less area[2]. The RCA with Cin=0 is also replaced with fast adders like CLA CSKA and CSA and analysis is done in terms of logic levels and delay.

II. PREVIOUS TECHNIQUES

A. *Carry select Adder (CSA):*

Carry select Adder (CSA) is one of the fastest adders used in many data processors to perform fast arithmetic functions. The carry select adder partitions the adder into several groups, each of which performs two additions in parallel using dual RCA's[4]. One copy evaluates the carry chain assuming the block carry-inis '0', while the other assumes it to be '1'. Once the carrysignals are finally computed, the correct sum and carry-out
signals will be simply selected by a set of multiplexers [4]
An example for carry select addition with carry input '0' and Carry -in '1' is shown below
1010 1010 1011 1111
0000 0011 1111 1010 (Cin=0)

(sum): 1010 1110 1011 1001
Cout='0'
1010 1010 1011 1111
0000 0011 1111 1010 (Cin =1)

Sum: 1010 1110 1011 1111

Cout='0'

B. *Modified carry Select Adder (MCSA)*

In Carry Select Adder more area is occupied because of dual Ripple Carry Adders (RCA) and also carry-out at every stage must ripple[4].So in order minimize delay caused by one of the RC Awhose carry input is '1' and to optimize area one RCA isreplaced with Binary to Excess-1 Converter (BEC), by which gate count will be reduced by a very large amount and computational time is optimized when compared to restof the adders as discussed above. Depending upon the carry out bit of the previous stage thesum is selected either from RCA or BEC with the help of2x1 multiplexer's at each stage.[5] An example of MCS Operation is shown below by randomly considering input bit stream.
1010 1010 1011 1111
0000 0011 1111 1010 (Cin=0)

Sum: 1010 1110 1011 1001

1010 1110 1011 1111 (BEC)
1 1 1 1010 (cin='0')

Sum: 1011 1111 1010 1111

From the above example we observe that even afterreplacing RCA's with carry input '1' with BEC there is nochange in carry output and sum.

C. MCSA with CLA

This architecture is similar to 16-bit Modified Carry Select Adder, the only change is that we replace Ripple Carry Adder with Carry Look-ahead Adder with Cin=1 along with BEC [5]. As the delay of 4-bit Carry Look-ahead Adder is more when compared to 4-bit Carry Skip Adder.

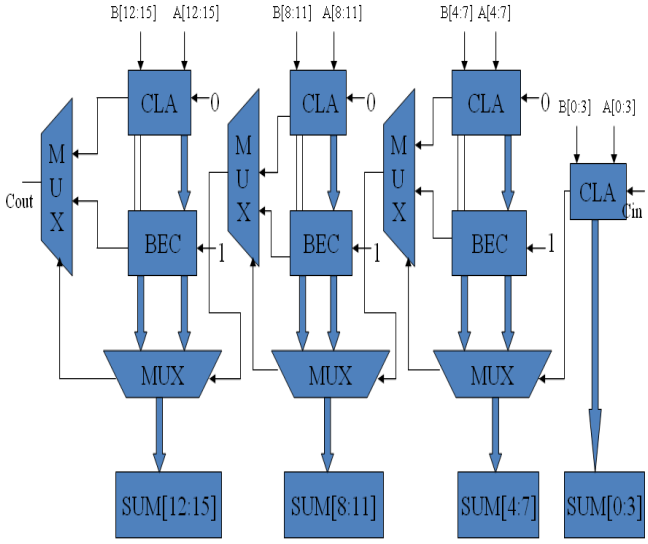

Fig 1: 16-bit MCSA with CLA

D. MCSA with CSA

As the delay in 4-bit Carry Look-ahead Adder is more whencompared to 4-bit Carry Skip Adder because of that reasonwe are replacing 4-bit Carry Look-ahead Adder with 4-bitCarry Skip Adder in order to reduce the delay and powerconsumption with minimum speed penalty.

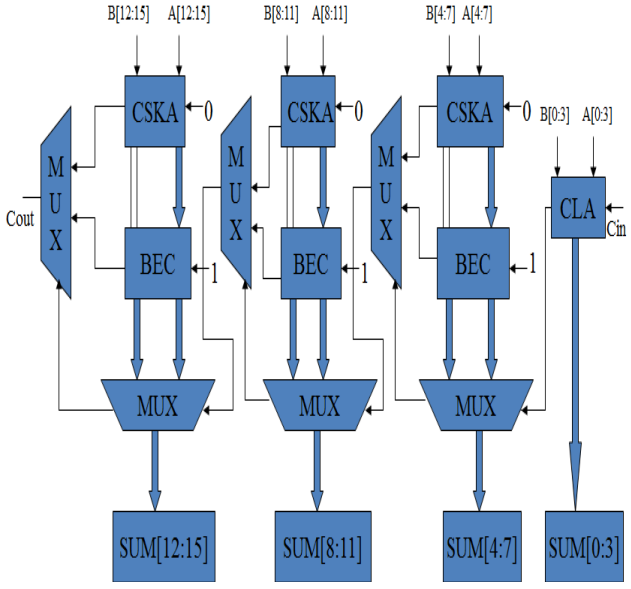

Fig 2: 16-bit MCSA with CSA

E. Regular SQRT CSLA

The basic square-root Carry Select adder has a dual ripple carry adder with 2:1 multiplexer, themain disadvantage of regular CSLA is the large area due tothe multiple pairs of ripple carry adder[5]. The regular 16-bitSQRT Carry select adder is shown below

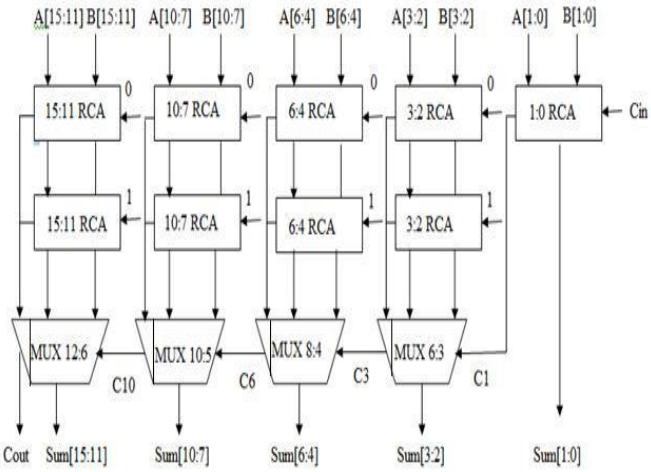

Fig 3: 16-bit SQRT with CSLA

III. Regular SQRT CSLA with BEC

The modified 16-bit SQRT CSLA using BEC is shown in Figure below. The structure is again divided into five groupswith different sizes of Ripple carry adder and BEC Theparallel Ripple carry adder with Cin=1 is replaced with BEC[6].One input to the multiplexer goes from the RCA with Cin=0and other input from BEC. Comparing the individual groupsof both regular and modified SQRT CSLA, it is clear that theBEC structure reduces delay[6]. But it is clear that ripple carryadders still result in carry propagation delay.

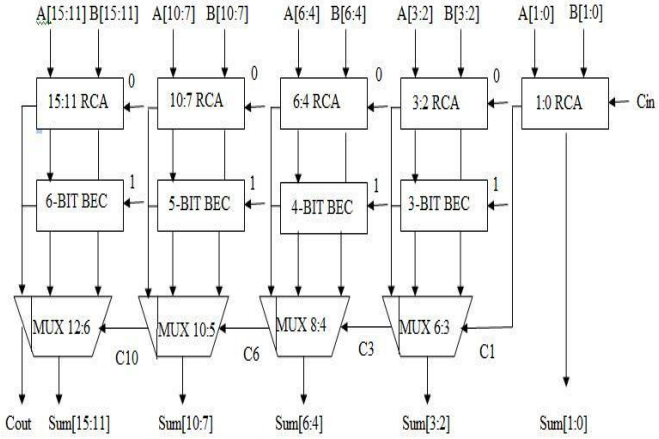

Fig 4: 16-bit Modified SQRT with BEC

IV. WORK DONE

For designing more area and speed efficient adder the Ripple Carry Adder in Modified Square root Carry Select Adder is replaced with fast adders. In order to know the efficient adder that can possibly replaced with RCA an analysis done on

Modified SQRT CSLA by replacing RCA with CLA, CSKA, Carry save adder[8]. The results are shown for all fast adders. First in MCSA the RCA is replaced with CLA and the waveforms are shown below. And from the synthesis report it is observed that area delay and log levels are reduced.

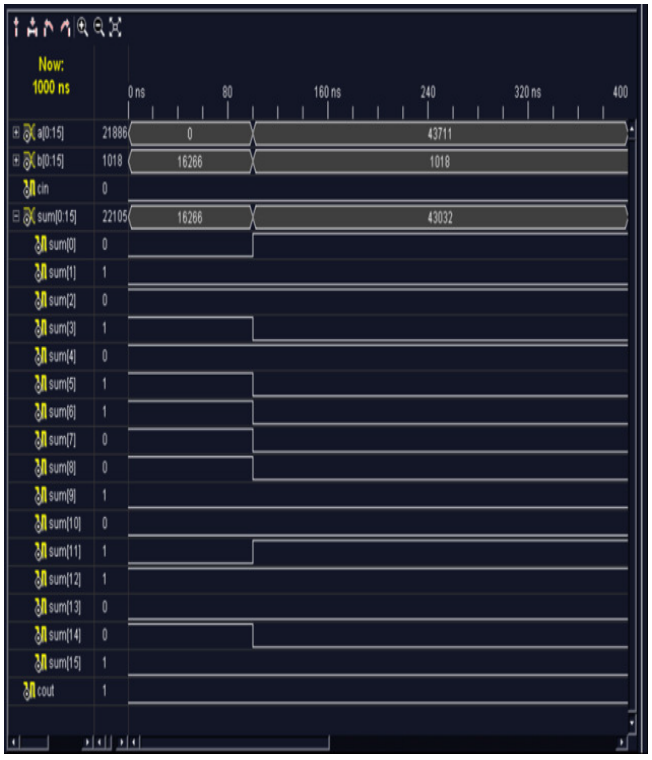

Fig 5: Output waveforms of 16-bit SQRT MCSA with BEC

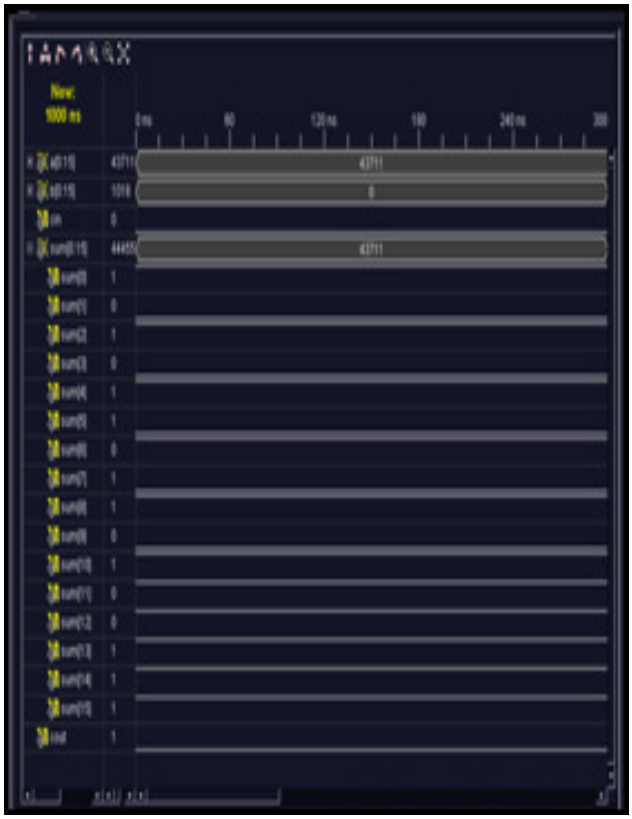

Fig 6: Output waveforms of 16-bit SQRT MCSA with CSKA

It is observed that delay and number of logic levels for evaluation of final carry output are still reduced when replaced with CSKA compared with CLA[[7]8]. For getting further optimized results CSKA is replaced with Carry Save Adder and the waveforms are shown below.

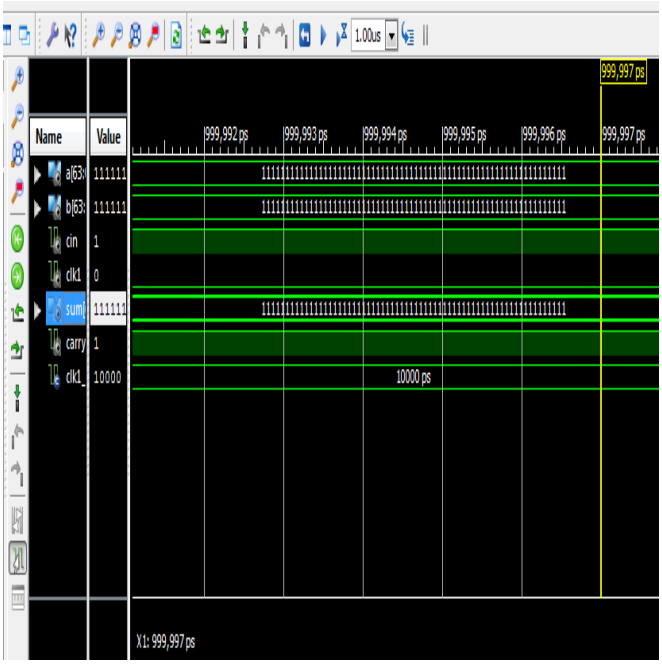

Fig 7: waveform of 16-bit SQRT MCSA with Carry save Adder.

It is inferred that SQRT MCSA with carry save adder gives better result.

V. CONCLUSIONS

In this paper three new architectures are presented for SQRT MCSA (Modified Carry Select Adder). Comparisons are made between different adders in terms of logic levels and delay. The proposed full adders show good performance and among the proposed SQRT MCSA's, MCSA with carry save adder show much optimized results.

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