Low Error Down Sampling Filter for Mobile System

Abdulhassan Nasayif Aldujaili

Abstract: ***This paper present, the design and simulation of decimation filter to work with wireless mobile system under software defined radio (SDR) technology. The decimation filter is designed with three stages of decimation filter that consists of Cascaded Integrated Comb (CIC) decimation filter, Compensating Finite Impulse Response (CFIR) filter and Programmable Finite Impulse Response (PFIR) filter. The three cascaded filters could operate to reduce the intermediate frequency from 100MHz to 100 KHz baseband signal in order to more processing. System Generator offers the multiplier less Multiply-Accumulate (MAC) Finite Impulse Response block which reduce the implementation area. The three filters has been verified in investigated by mean of fixed point and floating point values using matlab 7.4 and Xilinxe Sys. Gen. The simulation and verification results achieved minimum error of approximately*** $2x10^{-4}$***. Therefore, the introduced techniques support the current and future wireless generation in intermediate frequency up to 100 MHz.***

Keywords: Decimation Filter, SDR, MATLAB, System Generator

I. INTRODUCTION

In radio communication systems design, the low pass sample IF signal is obtainable to develop the presentation of Analog-Digital Converter (ADC). The purpose of digital front end in transceiver is to decrease the volume and power consumption and facilitate it to have reconstruction capability comparing with analog front end. A complete digital IF demodulation has the benefit to better performance and correctness. Though, with higher sample rate, it's important to decrease the frequency and sample rate in IF band via decimation filter in order to minimize the energy to lowest level in the in hand processor[1]. Since wireless communication infra structures have been introduced such as 3G and 4G, Software Defined Radio (SDR) becomes dominant due to its highly configurable hardware and software platforms, as compared to the sophisticated and complicated hardware platforms. Indeed, SDR performs many sophisticated signal processing tasks, e.g. channel estimation, rake receiving, and advanced compression algorithms. There are many silicon solutions for implementing the various functions of SDR, but Field Programmable Gate Array (FPGA) offers the best solution in data rate conversion processing because of its high level of integration (functionality), high performance (speed), high programmability, shorter development cycle, and low development costs [2]. In many SDR systems, decimation part is one of the prevalent methods for data rate conversion. The SDR offers high organize for a diversity of modulation techniques, wide band or narrow band operation. The compensation of SDR systems over conventional wireless communication systems are the flexibility and permit to numerous communication protocols to dynamically performs on the same hardware, thus reducing the cost. Specific functions such as filters, modulation schemes, encoder/decoder could be reconfigured adaptive at run time[3]. This will considerably decrease the cost of the system for both the end user and the service. The essential idea following the software radio is that the analog to digital converter is moved as closed as possible to the antenna and mainly function are realized by digital signal processing. For this reason, the A/D converter operates on extremely high sampling rate. The most important idea of the digital radio receiver is to convert the radio frequency signal into digital baseband signal. This type of receiver could be performed in three stages, convert the radio frequency signal into IF signal digitalized and demodulate it to baseband. This paper discusses the steps to design the decimation filter in the manner of Digital Signal Processing (DSP) by using Matlab/Simulink software [4].

To overcome the aliasing phenomena during sampling process, the new technique of data rate change should be used. Therefore, if high change in the sampling frequency is required, then the decimation with multi stage were constructed and become necessary [5]. Compared to one stage decimation, the filter response gave more stable and relaxing output. However, a lowpass filter could be inserted in filter whichever filter side in decimation process. Many advantages in the gain saving will obtained and the computation could minimize. The Nyquist conditions is required when incoming signal is oversampled. However, when the single stage decimator is used, this will increase the filter cost in the filtering term. In order to implement efficient technique in decimation stage, the multi phase design should used to provide best filtering process. In this case, the amount of multipliers might minimize also [6]. The conservative down sampling filter structure shown in Figure 1 could be capable to convert an intermediate frequency band into baseband signal using mixer in the digital region and 2 low pass filters after the A/D converter[7]. In this study, the cascaded integrated comb (CIC) decimator is used with compensating finite impulse response (CFIR) and programmable finite impulse response (PFIR) filters as cascaded decimation filter structure to convert the intermediate frequency to baseband with multiplier less MAC filter available with Xilinx products in order to decrease the

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multiplications processes. However. The implementation of this decimation filter will consumes less power and decrease the filter size to minimum. As an example, assume the proposed decimator filter is designed to work with GSM mask frequency as well as CDMA system.

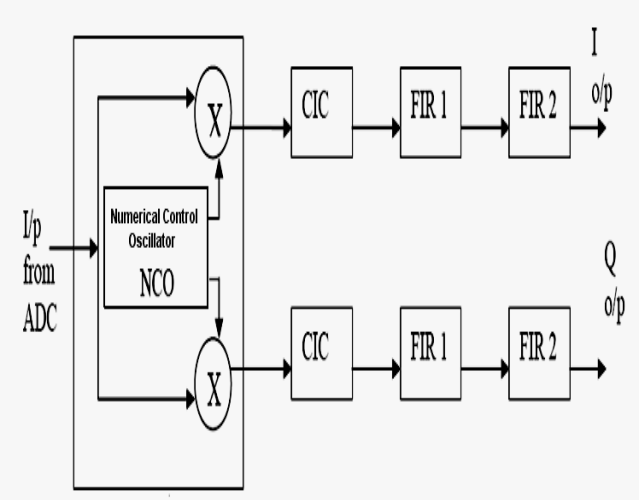

Figure 1: Conventional decimation Filter

II. DOWN SAMPLING FILTER STRATEGY

The Suggested down sampling filter prototype is constructed using matlab 7.4 and confirmed with fixed-point values of the filter presentation in the Xilinx product. Figure 2 illustrate the filter design in Simulink / matlab environments. The chirp signals is used to represent the IF band in GSM systems with 69 MHz. The proposed decimator is used to down sample the income signal from IF to baseband as well. The suggested decimator achieves and minimize the sample rate from intermediate frequency of GSM signal into baseband with no error occur and this signal has been prepared for demodulation process. The algorithms values in the filter represented in blocks parameters has been improved and modified to enable and promises filter structure in matalb. The output waveforms of all stage shows perfect similarity with original GSM wave as shown in Figure 3.

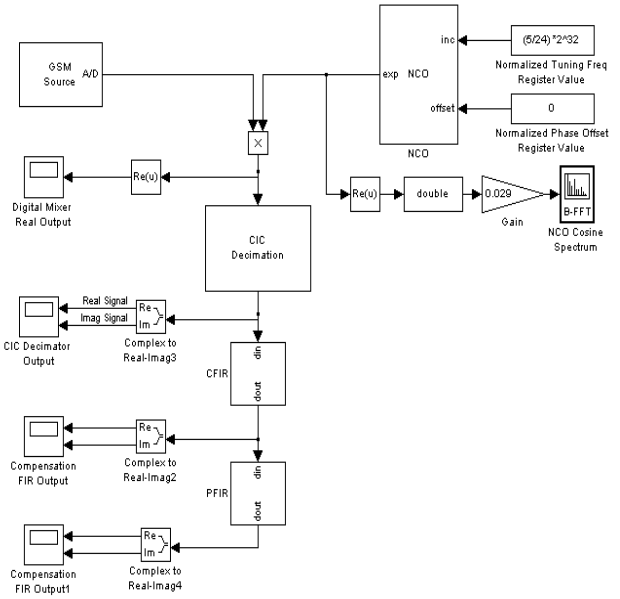

Figure 2: Matlab modules of suggested decimator

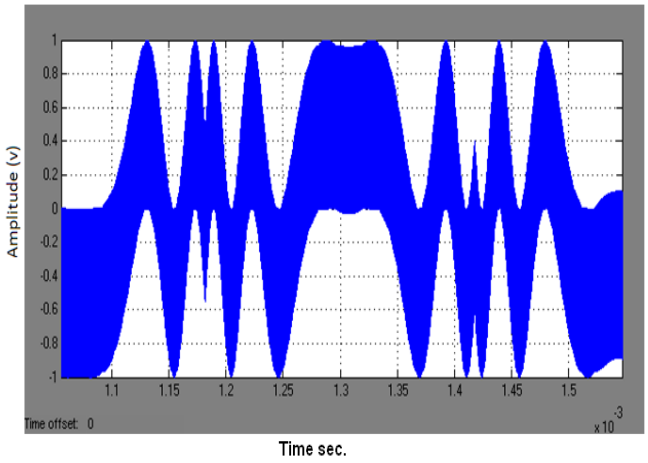

Figure 3: Decimator input signal

2.1. First Stage CIC Filter

The first stage represented by 5-stage CIC filter is designed with 64 down sampling factor to isolate the origin signal from IF band. Figure 4 shows the output waveforms of the first stage with 1.088 MHz frequency band and the gain of 2^{30} is gotten. Additionally, the magnitude value kept at ±0.5 meaning that the waveform rate is lower than IF band by 32 times.

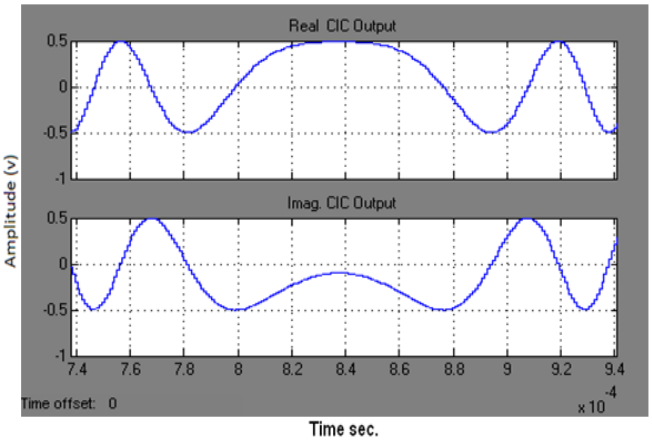

Figure 4: waveform output of first stage

2.2. Compensating Second Stage Structure

In the second stage of suggested filter, the new FIR filter is used with multiple accumulator technique from Xilinx product as illustrated in Figure 5.

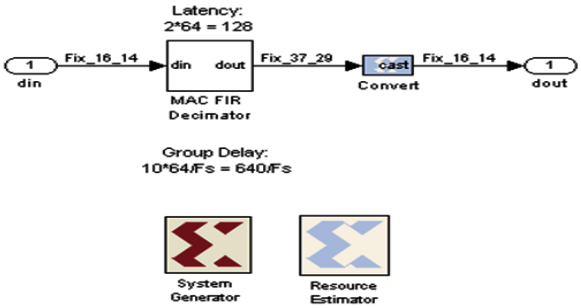

Figure 5: MAC CFIR Decimator

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In the system generator from Xilinx product, the multiplier less MAC block has been used to build the second stage in suggested decimator filter. To improve the filter response, the equiripple method in low pass filter is used to provide specific envelope output as GSM waveform. A 21-taps filter length and 1.08 MHz is adjusted to get exact sampling duration. Hence, 64Ts produce 923.0781 ns as required to fulfils the timing condition in matalb block set. The filter request shows exact linearity in the phase as illustrated in Figure 6. The magnitude response of this stage show stable behavioral and the pulse shaped waveforms is appear more close to GSM mask.

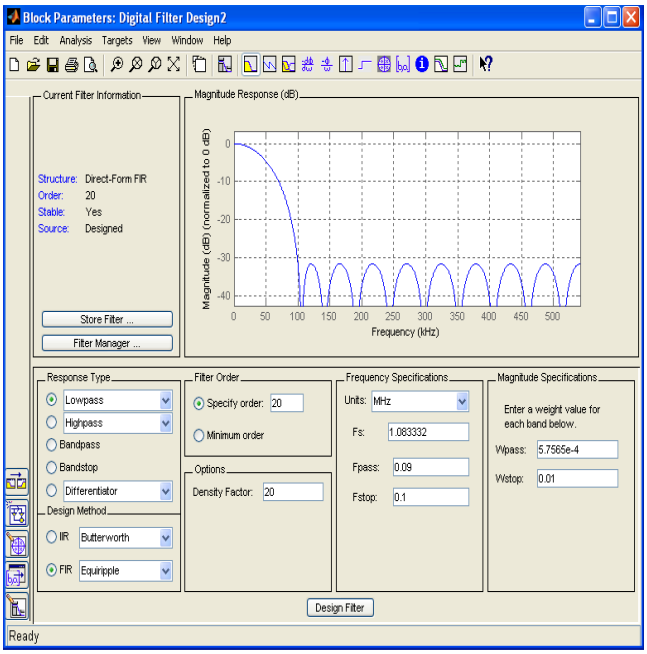

Figure 6: MAC filter output waveforms

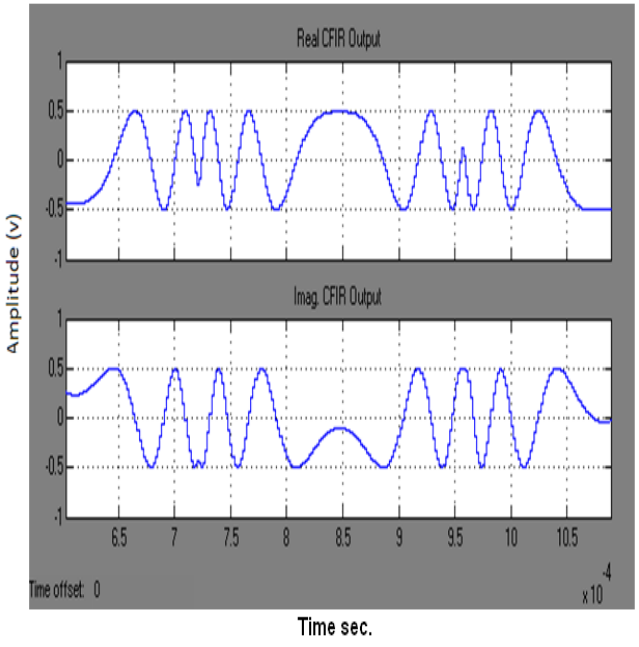

Figure 7: GSM mask waveforms for second stage output

2.3. Programmable Third Stage Structure

The programmable MAC FIR filter offered by Xilinx is used to build the third stage and verified with matlab design earlier apply to real time phase. Figure 8 shows the filter structure with the fixed point values for filter inputs.

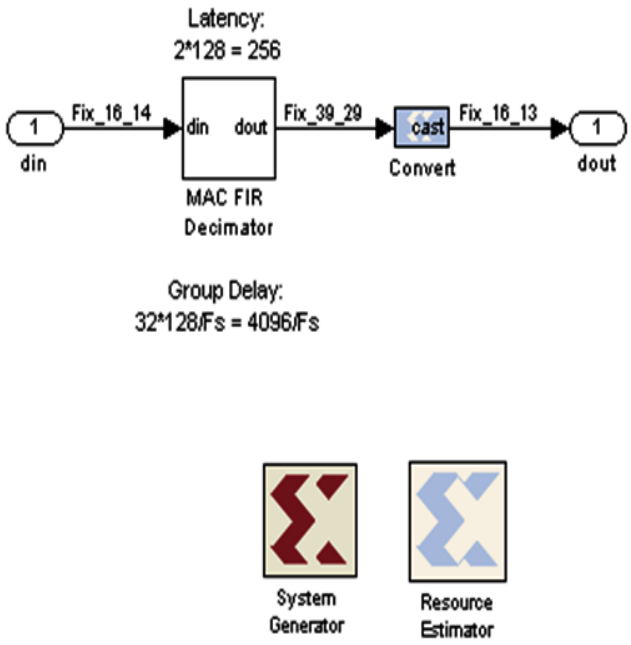

Figure 8: system generator design for third stags

The system generator blocks is used to design the third stage programmable lowpass filter with equiripple methods. Hence, the 65-taps filter length is applied and frequency is adjusted to be 541 MHz. Therefore, the sampling duration should satisfy the timing condition as 128Ts= 846 ns and the drop frequency 80 kHz. The filter request provide the interest band of GSM system with linear phase in the required band as shown in Figure 9. The envelope waveform of output signal for third stage look like GSM mask exactly as illustrated in Figure 10.

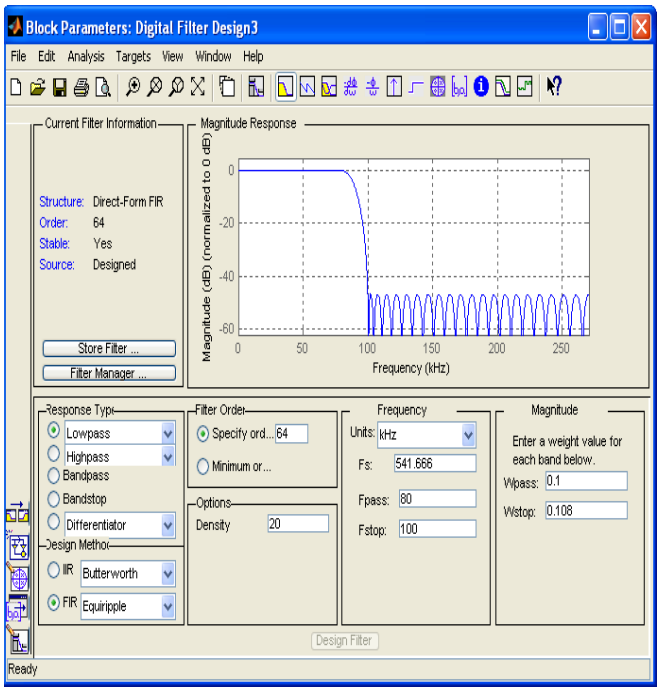

Figure 9: third stage filter response

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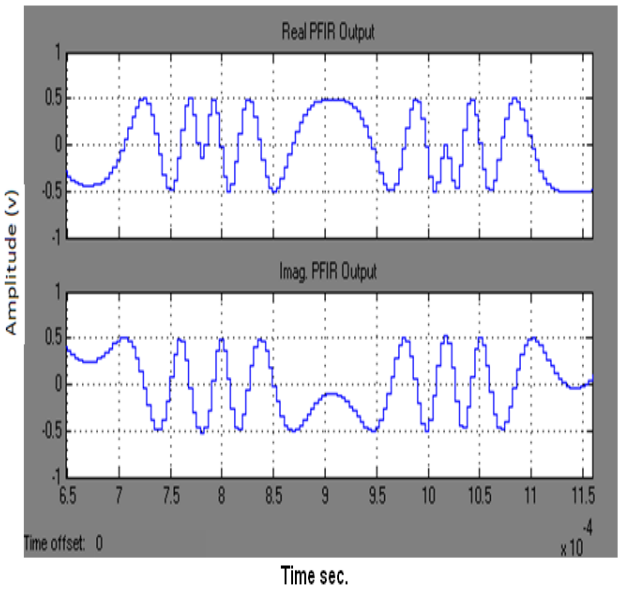

Figure 10: third stage output waveforms

III. PROPOSED FILTER CONFIRMATION

The suggested decimator is verified with ideal DDC filter to show the different between the two filter response and performance in each stage. Figure 11 shows the verification design using system generator subsystems connected in parallel and ruining with same input. The original input waveform and the output waveforms of ideal and proposed filter is compared using time scope as illustrated in Figure 12. As clear from the output waveforms, the different between two filter is less than 2×10^{-4} and this values still accepted due to quantization error.

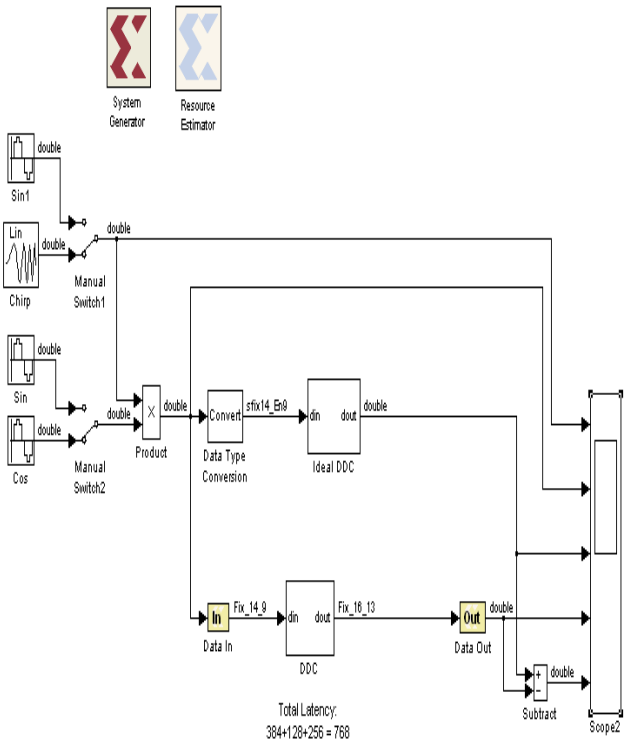

Figure 11: parallel connection between ideal and suggested decimator

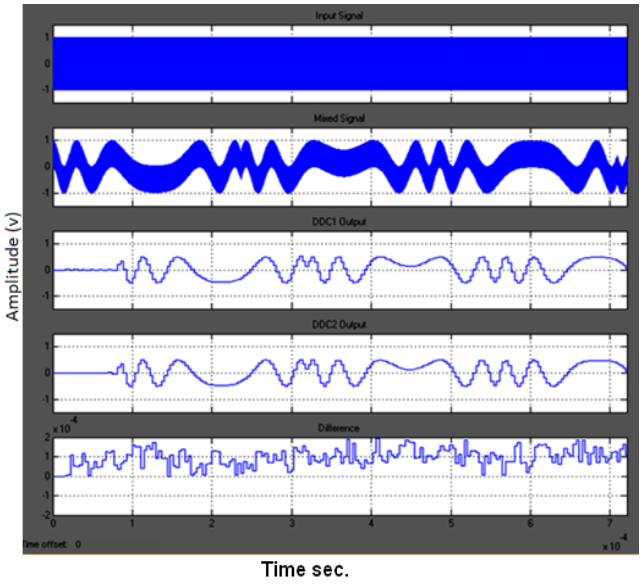

Figure 12: output waveforms of ideal and suggested decimator

IV. CONCLUSION

In current wireless and mobile systems, it's desired to design efficient and minimum cost equipment due to user demand in the small size and long life device. The decimation stages in the mobile receiver consider as the most part in the power consumption and size minimization. Hence, in this paper, many new software has been used to facilitate the suggested design with minimum error. To provide a tradeoff among complexity and number of stages in the suggested frequency decimator, the MAC product from Xilinx is used as the best multiplier less filter. The suggested filter promising for current and future mobile generation with further tuning in the number of stages and type of filter method design to achieve better performance.

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AUTHORS PROFILE

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