

Synthesis of Effect of Self Heating Effect on Electrical Characteristics in SOI MOSFET

Jyoti Kumawat, Mukesh Kumar Yadav

Abstract: This article describes the use of silvaco TCAD tools to develop SOI MOSFET technology and device simulation results. The purpose of this simulation is to investigate the effect of self heating effect on the electrical properties of the device. The results show that the impact of self heating phenomenon on the Id-Vd curve. The device was manufactured using ATHENA software, and the simulation was done with the help of ATLAS software. All charts were made using Silvaco. We briefly introduce SOI MOSFETs Transistors and problems at high temperatures Self-heating effect, and then we present the simulation results get related using the SILVACO TCAD tool SOI n-MOSFET structure. We will also show some of the simulation results we have obtained The effect of temperature changes on our structure directly affect its drain current.

Keywords: SOI technology, SOI MOSFET, Self-heating effects, Silvaco Software, Silicon-On-Insulator, MOSFET, Silvaco, ATHENA, ATLAS.

I. INTRODUCTION

J.E Lilienfield obtained the first patent concept of field effect transistors, "the method and device to control the current" almost 80 years ago; It evolved into a modern metal oxide semiconductor field effect transistor MOSFET. He proposed a three-terminal device in which the source-to-drain current is controlled by the field effect of the gate and is dielectrically insulated from the rest of the device. The active part of the device is built on a thin semiconductor film deposited on the insulation. Either coincidentally, the first proposed FET is in fact an SOI device. The concept of this proposal is regrettable and soon forgotten, because the concept is too fictitious and cannot be produced by the technology of the time. When the bipolar transistor became successfully main stream in the 1940s, the concept of field effect transistor lost its position even further.

SOI devices have the advantage of fast speeds of 20% to 30% and consume one-third to half the power of MOSFETs. In addition, the reduction in voltage of the power supply seems to give SOI a good opportunity to incorporate conventional technology. However, due to immature wafers, these advantages are still insufficient to treat SOI as a production technology level. The following are the same ones that "technical infrastructure and circuit design is inadequate." In 1965 Gordon Moore introduced a well-known Law This bill describes the evolution of transistor density in integrated circuits. The prediction is that the number of transistors per chip increases four times every three years.

Revised Version Manuscript Received on July 28, 2017

Jyoti Kumawat, M.Tech Scholar, Rajasthan Technical University, Kota (Rajasthan), India.

Mukesh Kumar Yadav, Assistant Professor, Sri Balaji College of Engineering and Technology, Jaipur (Rajasthan), India.

The development of industry technology follows Moore's law of The last 40 years. Silicon technology progressed faster every year. The main problem should be focused on silicon technology, the amount of silicon devices can be reduced, and what is the effect of reducing the size of the device. By actively scaling the size of the semiconductor device, the complexity of the circuit has increased. When there is a silicon metal oxide (MOSFET) semiconductor field effect transistor having a gate size up to the deep submicron region, there are many serious problems with standby power consumption of the ultra-large-scale integrated circuit (ULSI). One of the most important problems to overcome is the source / drainage bond formation technique, which avoids the short channeling effect of nanoscale devices. In order to overcome this problem, new circuit design techniques have been introduced for new technologies such as silicon on insulation (SOI).

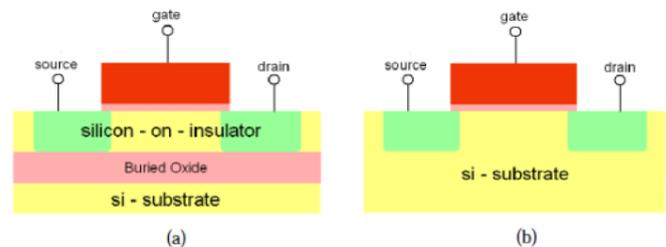


Fig-1 Structure of SOI-MOSFET

As the expansion continues to meet market needs, conventional bulk silicon devices are now subject to some basic physical limitations for further scaling. It is believed that silicon-on-insulator technology can be a good alternative to conventional MOSFETs in deep submicron regions. However, the tolerance of partially and completely depleted SOI MOSFETs remains a problem.

II. SOI MOSFET TRANSISTOR

SOI (silicon on insulator) was originally invented for use in many special environments, such as radiation hardening or high voltage integrated circuits. In recent years, SOI has become a serious competitor for low power and high performance applications [2]. SOI MOSFETs are different from traditional high-capacity MOSFETs. For bulk MOSFETs, the silicon channel region is directly on the substrate. For the SOI MOSFET, a buried oxide layer is formed on the bulk silicon substrate. The silicon thin film is present on the top of the buried oxide layer in which the active MOS device and the circuit are provided. The cross section of the basic n-type MOSFET on the SOI is shown in Fig.



Synthesis of Effect of Self Heating Effect on Electrical Characteristics in SOI MOSFET

Figure 2 shows a photograph of an example of a SOI MOSFET. Fig. 2 (a) Fig. 1 is shown in Fig. Figure 2 (b)

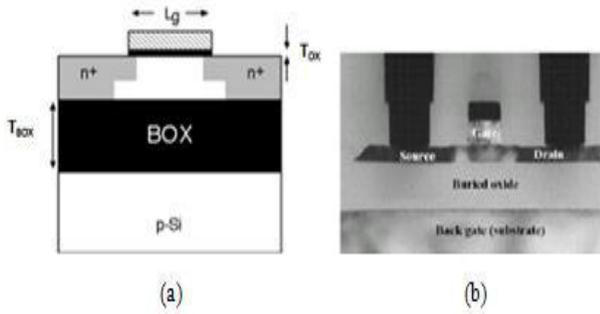


Fig-2 Cross Section structure of SOI-MOSFET

SOI MOSFETs have many advantages over devices and circuit stages. Due to the buried oxide (BOX) layer, the parasitic capacitance of the SOI MOSFET device is less than the parasitic capacitance of the MOSFET. Thus, the use of SOI MOSFETs can increase the speed of digital CMOS circuits to reduce the latency of digital CMOS circuits due to junction capacitance. On the other hand, the power delay of the SOI CMOS circuit is much smaller than that of the bulk symmetry, which is also due to the smaller parasitic capacitance in the SOI MOSFET and the reduced leakage current through the BOX. So we can say that SOI MOSFET technology has high speed and low power characteristics. On the device side, the SOI MOSFET is not latched due to buried oxide isolation, and compared to bulk MOSFETs, SOI MOSFETs are more susceptible to isolating devices, making SOI CMOS technology with higher device densities and easier device isolation structures. While these advantages of SOI technology are well known, the successful introduction of SOI technology for large-scale applications faces some key challenges in the entire range of materials, processes, manufacturing and devices, design. SOI manufacturing process is changing Mature enough to mass production of low cost, low defect density of the substrate. Another major problem is to control the thickness of the silicon film to precisely control the threshold of fully depleted devices.

The SOI MOSFET can be further divided into partial depletion (PD) and fully depleted (FD) SOI devices. In addition, components with thin SOI layers (typically <50 nm) and all body regions under the channel are depleted are called fully depleted SOIs. In contrast, elements that have a thick SOI layer (typically > 100 nm) and that are not depleted in the bottom of the body region are referred to as partially depleted SOI [5].

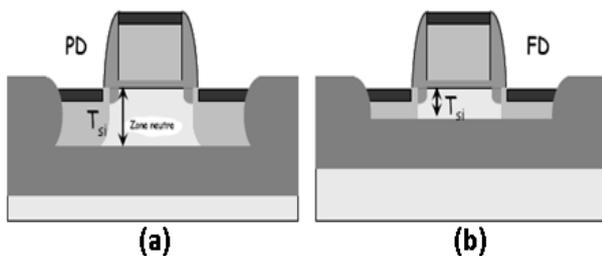


Fig. 3 (a) Structure of partially depleted SOI MOSFET, (b) Structure of fully depleted SOI MOSFET

III. DEVICE SIMULATION

Numerical simulations of the SOI n MOSFET were performed by using the SILVACO TCAD tools. The different parameters of our structure are assumed as follows:

Table-1 (List of Parameters)

Symbol	Designation
LD,LS,LG	Drain length, Source length and Gate length
L	Channel length
TOX	Gate oxide thickness
Tsi	Silicon film thickness
TBOX	Buried oxide thickness
	substrate thickness
	Depth junction
NA	Substrate concentration
ND	Drain and Source concentration

The below structure is obtained using ATLAS device simulation using. The thickness of the silicon film is 0.2 um. This ensures that the channel is partially depleted.

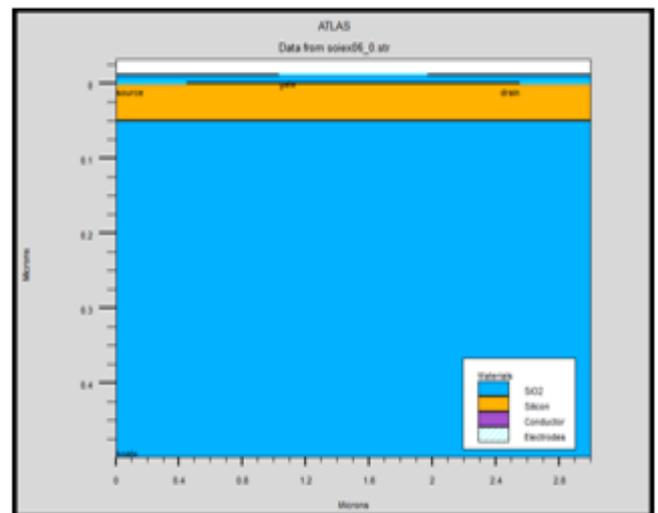


Fig.4. SOI-MOSFET Structure

IV. SELF HEATING EFFECTS

The operation of the MOSFET transistor, the electric power generates a quantity of heat per Joule effect. More the power will be raised; the temperature of the channel will increase. However, the physical parameters such as mobility, the threshold voltage or the saturation speed are temperature dependent. These three parameters are related to the temperature by the following empirical relations

$$\mu_{eff} = \mu_{eff, Tamb} (T/T_{amb})^{-k_1}$$

$$V_{th} = V_{th, Tamb} - k_2 (T - T_{amb})$$

$$V_{sat} = V_{sateff, Tamb} - A_T [(T/T_{amb}) / T_{amb}]$$

Where: $k_1 \in [1, 5 ; 1, 7]$, $k_2 \in [0, 5 ; 4]$, $A_T = 3, 3 \cdot 10^4$.

The reduction of effective mobility is dominated by restrictive factors. When the temperature or dissipation power increases, the decrease in mobility involves a decrease in the drain current IDS. Therefore, the power dissipated will be lower, which will involve a decrease in temperature. Then build self-sustaining phenomena, connect channel temperature and IDS. It is self-heating effect.

Depending on the type of material and its thermal conductivity, the heat generated will be discharged through the entire device. The final amount varies linearly according to temperature. Therefore, in the case of a MOSFET including a buried oxide as compared with a counterpart on the bulk silicon, the heat generated is difficult to discharge. This insulation involves an increase in the temperature in the channel. Thus, the effect of the self-heating effect in the SOI MOSFET transistor is more pronounced.

V. SIMULATION AND RESULTS

Figure 5 and Figure 6 shows the $I_{DS}-V_{DS}$ characteristics of the SOI-MOSFET transistor for 3V gate bias, respectively. The current drain IDS decreases as the temperature increases. At high temperatures, the channel mobility is reduced. This reduction in mobility results in a reduction in drain current.

The dependence of the drain current IDS on temperature is affected by the threshold voltage and the channel mobility $I_D(T) \approx \mu(T) [V_{GS} - V_{th}(T)]$. The reduction of these two parameters has the opposite effect on the current.

The $[V_{GS} - V_{th}(T)]$ term causes the drain current to increase as the temperature increases, because the threshold voltage decreases with temperature. On the other hand, the $\mu(T)$ term causes the drain current to decrease as the temperature increases, since the lattice scattering dominates at high temperatures and leads to a decrease in channel mobility.

At the high gate bias, the $\mu(T)$ term is dominant and the $[V_{GS} - V_{th}(T)]$ term is dominant under the low gate bias [1].

In a given temperature beach, the current I_{DS} does not vary with the temperature of the gate bias V_{GS} called V_{GS} (ZTC) (zero temperature coefficient).

In addition, we can see the advantages of SOI technology, which exhibits a ZTC point over a wide temperature range of up to 600K. Simulation is able to identify the ZTC bias point [1] of the bulk CMOS transistor in linear and saturation regions up to 200 °C.

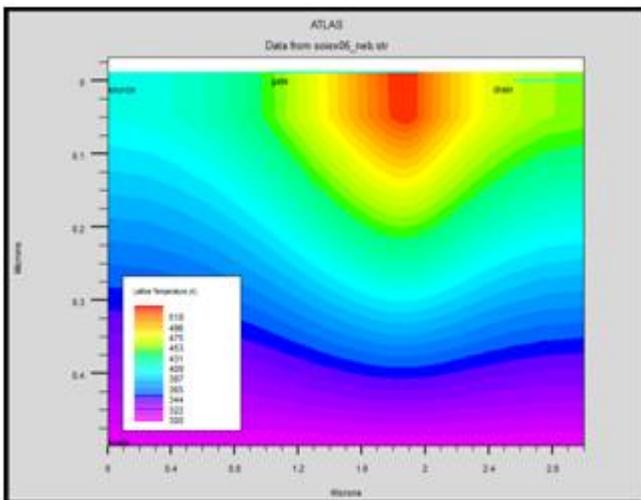


Fig.5 Lattice Temperature in SOI MOSFET

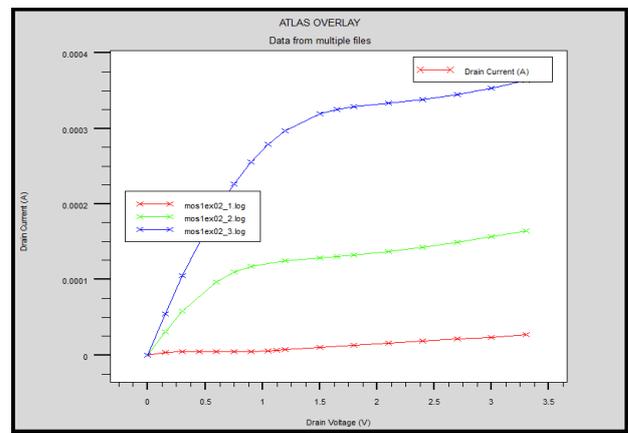


Fig.6 I_D-V_D Characteristics of SOI MOSFET without Self Heating

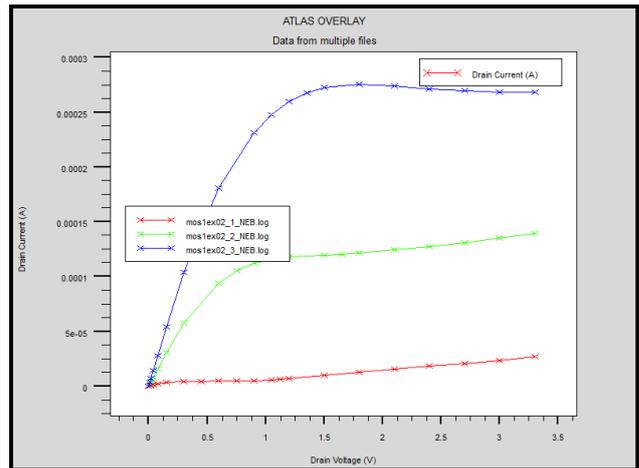


Fig.7 I_D-V_D Characteristics of SOI MOSFET with self heating

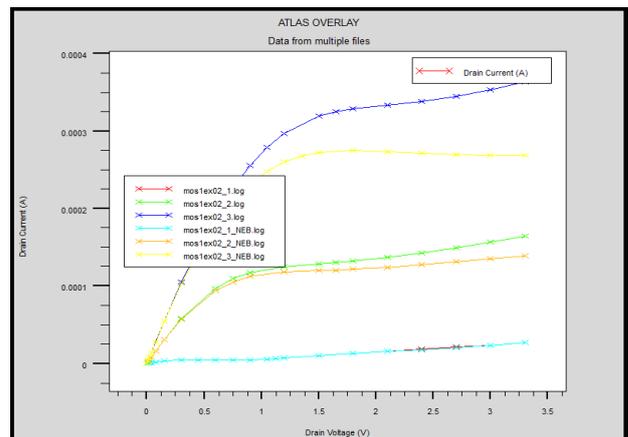


Fig.8 I_D-V_D Characteristics of SOI MOSFET with and without self heating

In the short channel devices, the potential barrier to form the conduction channel depends by both the transversal field (controlled by the gate-to-source bias) and the longitudinal field (controlled by the drain-to-source bias), at high drain bias, we see a lower ZTC bias point,

The potential barrier decreases leading to drain-induced-barrier-lowering (DIBL) that causes the threshold voltage to drop. Hence we see a lower ZTC bias point at high drain bias for a short channel SOI MOSFET.

VI. CONCLUSION

From the simulation results of the SOI n MOSFET structure working with the Atlas-SILVACO tool, we can note the following: Temperature is one of the basic parameters to be considered. In fact, the temperature makes it possible to change component performance and therefore Circuit. The use of CMOS devices on body substrates at high temperatures is limited by the presence of latches and high leakage currents.

The CMOS devices on the SOI substrate operate at high temperatures. Using this technique eliminates the latch, the leakage current is not important, which is for these SOI technology is highly exploited to a great extent Temperature application.

REFERENCES

1. A.K. Goel, T.H. Tan, High-temperature and self-heating effects in fully depleted SOI MOSFETs *Microelectronics Journal* 37 (2006) 963–975.
2. J. P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. Boston, MA: Kluwer, 1991.
3. Wei Ma thesis, Linearity Analysis of Single and Double-Gate Silicon-On-Insulator Metal-Oxide-Semiconductor-Field-Effect- Transistor, Ohio University, August 2004.
4. Alexandre SILIGARIS « Modélisation grand signal de MOSFET en hyperfréquences : application à l'étude des non linéarités des filières SOI » Thèse de doctorat 2004-UNIVERSITE DES SCIENCE ET TECHNOLOGIES DE LILLE.
5. <http://docinsa.insa-lyon.fr/these/pont.php?id=daviot>
6. G.K. Celler, S. Cristoloveanu, *Journal of Applied Physics*, Vol.93, no. 9, p. 4955,2003.
7. F.S. Shoucair, W. Hwang, Electrical characteristics of large scale integration (LSI) MOSFETs at very high temperatures part II: experiment, *Microelectron. Reliab.* 24(3) (1984) 497–510.
8. Cristoloveanu, Sorin. "Introduction to silicon on insulator materials and devices." *Microelectronic engineering* 39.1 (1997): 145-154.
9. Lim, Hyung-Kyu, and Jerry G. Fossum. "Threshold voltage of thin-film Silicon-on-insulator (SOI) MOSFET's." *Electron Devices, IEEE Transactions on* 30.10 (1983): 1244-1251.
10. Bergveld, P. "ISFET, theory and practice." *IEEE Sensor Conference Toronto*. Vol. 10, 2003.
11. Aydin, C., et al. "Double Gate Coupling and Quantum Tunneling in Ultrathin SOI MOSFETs." *Future Trends in Microelectronics*, Wiley & Sons (2004).
12. H. J. Jang, and W. J. Cho, "Performance enhancement of capacitive-coupling dual-gate ion-sensitive field-effect transistor in ultra-thin-body", *Scientific Reports* 4, 2014.